# SECTION 9

# ELECTRICAL SPECIFICATIONS

## 9.1    INTRODUCTION

This section contains the electrical specifications and associated timing information for the MC68HC05E0.

## 9.2    MAXIMUM RATINGS [†]

### Table 9-1. Maximum ratings

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | $-0.3$ to $7.0$ | V |
| Input Voltage | $V_{in}$ | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V |
| Operating Temperature Range | $T_A$ | $T_L$ to $T_H$ 0 to 70 | °C |
| Storage Temperature Range | $T_{stg}$ | $-65$ to $150$ | °C |
| Current Drain per Pin * Excluding $V_{DD}$ and $V_{SS}$ $V_{DD}$ (total through two pins) $V_{SS}$ (total through two pins) | $I_D$ | 25 100 250 | mA mA mA |

\*    One pin at a time, observing maximum power dissipation limits.

†    This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.  Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (eg. either GND or $V_{DD}$).

## 9.3   THERMAL CHARACTERISTICS AND POWER CONSIDERATIONS

The average chip junction temperature, $T_J$, in degrees Celsius can be obtained from the following equation:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

Where:

$T_A$ = Ambient temperature (°C)
$\theta_{JA}$ = Package thermal resistance, junction-to-ambient (°C/W)
$P_D$ = $P_{INT} + P_{I/O}$ (W)
$P_{INT}$ = Internal chip power = $I_{DD} \bullet V_{DD}$ (W)
$P_{I/O}$ = Power dissipation on input and output pins (user determined) (W)

Note:   For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is:

$$P_D = K + (T_J + 273°C)$$

Solving the equations $P_D$ and $T_J$ for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2$$

Where K is a constant pertaining to a particular part. K can be determined by measuring $P_D$ (at equilibrium) for known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving the above equations for any value of $T_A$. The package thermal characteristics are shown in Table 9-2.

**Table 9-2. Thermal Characteristics**

| Characteristics | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance<br>    Plastic 68-Pin Quad Pack (PLCC) | $\theta_{JA}$ | 50 | °C/W |

| Pins | R1 | R2 | C |
|---|---|---|---|
| A12 - A0,<br>PD7 - PD5,<br>$\overline{CSROM}$, R/$\overline{W}$,<br>$\overline{CS2}$, $\overline{CS3}$ | 3.26 k$\Omega$ | 2.38 k$\Omega$ | 50 pF |
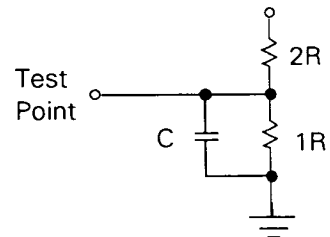


**Figure 9-1.  Equivalent Test Load**

**ELECTRICAL SPECIFICATIONS**

## 9.4 DC ELECTRICAL CHARACTERISTICS

$(V_{DD} = 5.0 \text{Vdc} \pm 10\%, V_{SS} = 0\text{Vdc}, T_A = 0 \text{ to } 70°C)$

### Table 9-3. DC Electrical Characteristics (5V)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Output Voltage (all output pins)<br>$I_{Load} = 10 \ \mu A$<br>$I_{Load} = -10 \ \mu A$ | $V_{OL}$<br>$V_{OH}$ | –<br>$V_{DD}-0.1$ | 0.1<br>– | V<br>V |
| Output Voltage (address bus and data bus)<br>$I_{Load} = 1.6 \text{ mA}$<br>$I_{Load} = -0.8 \text{ mA}$ | $V_{OL}$<br>$V_{OH}$ | –<br>$V_{DD}-1.4$ | 0.4<br>– | V<br>V |
| Input High Voltage | $V_{IH}$ | $0.5 \times V_{DD}$ | – | V |
| Input Low Voltage | $V_{IL}$ | $V_{SS}$ | 0.8 | V |
| Supply Current ($f_{op}$ = 4 MHz, $f_{osc}$ = 8 MHz)<br>Run<br>Wait<br>Stop | $I_{DD}$ | <br>–<br>–<br>– | <br>25<br>20<br>50 | <br>mA<br>mA<br>$\mu A$ |
| High- Z Leakage Current<br>(All input pins except $\overline{RESET}$ , PD5, PD6, PD7) | $I_{IL}$ | <br>– | <br>±10 | <br>$\mu A$ |
| Output High Source Current ($V_{OH}$ = 2.4 V)<br>Port A<br>Port B<br>Ports C, D, E and $\overline{CSROM}$ | $I_{OH}$ | <br>10<br>5<br>2.5 | <br>–<br>–<br>– | <br>mA<br>mA<br>mA |
| Output Low Sink Current<br>Port A ($V_{OL}$ = 0.4 V)<br>Port A ($V_{OL}$ = 1.0 V)<br>Port B ($V_{OL}$ = 0.4 V)<br>Port B ($V_{OL}$ = 1.0 V)<br>Ports C, D, E and $\overline{CSROM}$ ($V_{OL}$ = 0.4 V)<br>Ports C, D, E and $\overline{CSROM}$ ($V_{OL}$ = 1.0 V) | $I_{OL}$ | <br>8<br>24<br>6<br>16<br>1.6<br>4 | <br>–<br>–<br>–<br>–<br>–<br>– | <br>mA<br>mA<br>mA<br>mA<br>mA<br>mA |
| Input Current<br>$\overline{RESET}$ , PD5, PD6, PD7<br>INTX, OSC1 | $I_{in}$ | <br>–70<br>– | <br>–<br>±1 | <br>$\mu A$<br> |
| Capacitance<br>Ports (as input or output)<br>$\overline{RESET}$, INTX | $C_{out}$<br>$C_{in}$ | <br>–<br>– | <br>12<br>8 | <br>pF<br>pF |

Notes:  Wait $I_{DD}$: Only timer system active. If Serial Interface active add 10% to current drain.

Run $I_{DD}$, Wait $I_{DD}$: Measured using external square clock source (Fosc = 8 MHz), all inputs 0.2V from rail, no DC loads, maximum load on outputs 50pF (OSC2 load 20pF).

Wait, Stop $I_{DD}$: All ports configured as inputs , $V_{il}$ = 0.2V and $V_{ih} = V_{DD}$ - 0.2V.

Stop $I_{DD}$ measured with OSC1 = $V_{SS}$.

Wait $I_{DD}$ is affected linearly by the OSC2 capacitance.

## 9.5 AC ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 5.0V dc ± 10%, $V_{SS}$ = 0Vdc, $T_A$ = 0 to 70°C)

**Table 9-4. AC Electrical Characteristics (5V)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Frequency of Operation | | | | |
|    Crystal | $f_{osc}$ | – | 8.0 | MHz |
|    External Clock | $f_{osc}$ | dc | 8.0 | MHz |
| Internal Operating Frequency | | | | |
|    Crystal ($f_{osc}$ + 2) | P02 | – | 4.0 | MHz |
|    External Clock ($f_{osc}$ + 2) | P02 | dc | 4.0 | MHz |
| Cycle Time | $t_{cyc}$ | 250 | – | ns |
| Crystal Oscillator Startup Time | $t_{OXOV}$ | – | 100 | ms |
| STOP Recovery Startup Time (Crystal Oscillator) | $t_{ILCH}$ | – | 100 | ms |
| $\overline{RESET}$ Pulse Width | $t_{RL}$ | 1.5 | – | $t_{cyc}$ |
| Interrupt Pulse Width Low (Edge-Triggered) | $t_{ILIH}$ | 125 | – | ns |
| Interrupt Pulse Period | $t_{ILIL}$ | * | – | $t_{cyc}$ |
| OSC1 Pulse Width | $t_{OH}, t_{OL}$ | 55 | – | ns |

\* The minimum period $t_{ILIL}$ should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 $t_{cyc}$.
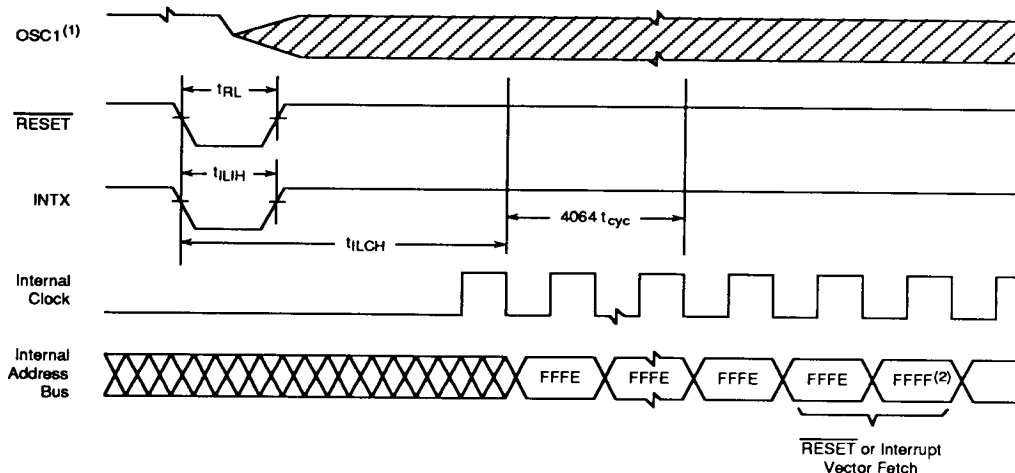
**NOTES:**
1. Represents the internal gating of the OSC1 pin.
2. RESET vector address shown for timing example.

**Figure 9-2. Stop Recovery Timing Diagram**

**Table 9-5. Expanded Bus Timing**

| Num | Characteristic | Symbol | Min | Typ | Max | Unit |
|-----|----------------|--------|-----|-----|-----|------|
| 1 | Cycle Time | $t_{CYC}$ | 250 | – | DC | ns |
| 2 | Clock Transition | $t_R$, $t_F$ | – | 10 | 25 | ns |
| 3 | Read/Write Hold | $t_{RWH}$ | 0 | – | – | ns |
| 4 | Address Hold | $t_{AH}$ | 0 | – | – | ns |
| 5 | Read/ Write Delay | $t_{RWD}$ | – | – | 25 | ns |
| 6 | Address Delay | $t_{AD}$ | – | 40 | 75 | ns |
| 7 | Data Set-up (MPU Read) | $t_{DSR}$ | 40 | – | – | ns |
| 8 | Data Hold (MPU Read) | $t_{DHR}$ | 0 | – | – | ns |
| 9 | Data Delay (MPU Write) | $t_{DDW}$ | – | 60 | 100 | ns |
| 10 | Data Hold (MPU Write) | $t_{DHW}$ | 20 | – | – | ns |
| 11 | Chip Select Hold | $t_{CSH}$ | 0 | – | – | ns |
| 12 | Chip Select Delay | $t_{CSD}$ | – | – | 25 | ns |
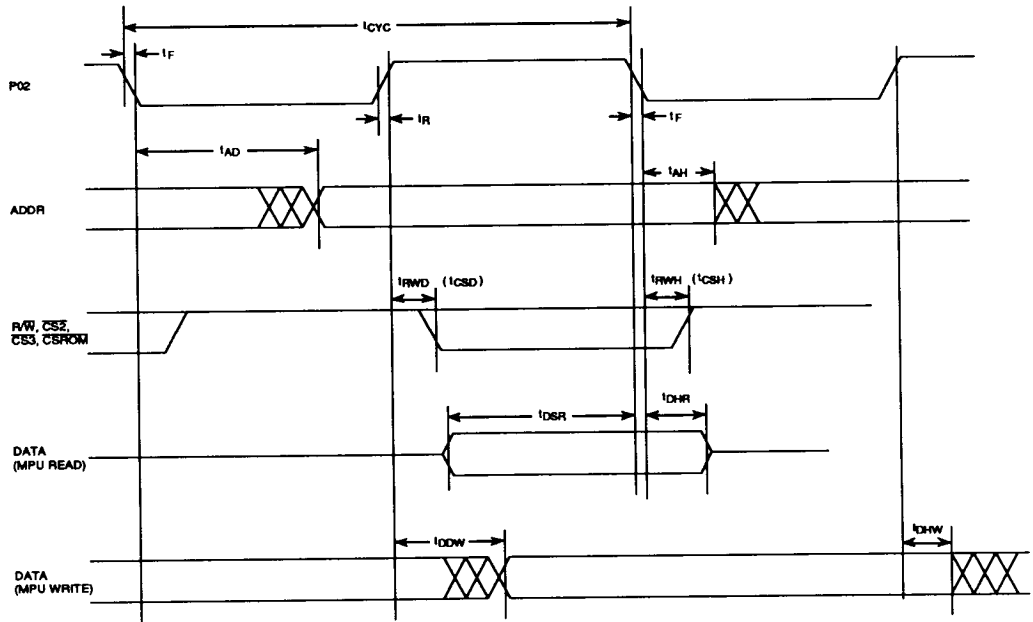
**Figure 9-3. Expanded Bus Timing Diagram**

**ELECTRICAL SPECIFICATIONS**

MC68HC05E0

## 9.6 SERIAL INTERFACE TIMING
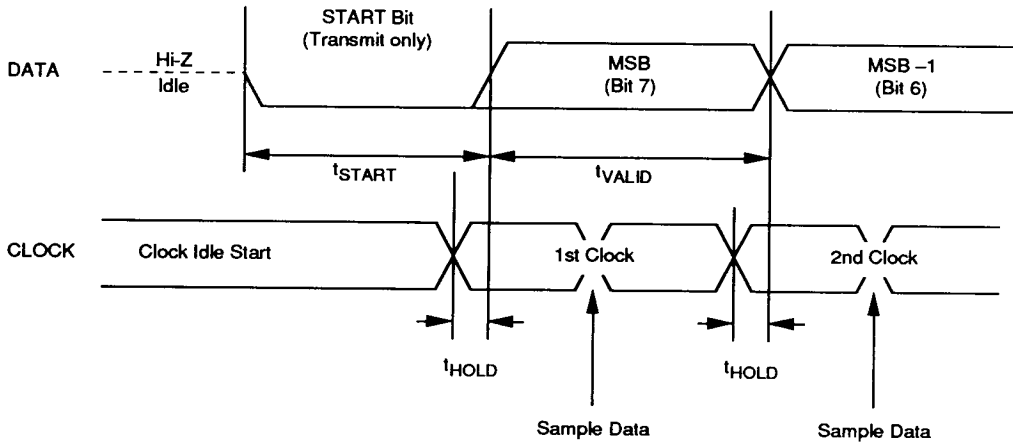


$t_{HOLD}$ = 1 Bus Cycle Time + $t_{pd}$      ($t_{pd} \approx 0 \rightarrow 30$ ns)

$t_{START}$ = $t_{VALID}$ = 1/SPI Transfer Frequency      (SPI Transfer Frequency determined by BD0/BD1)

**Figure 9-4. SPI Timing Diagram**
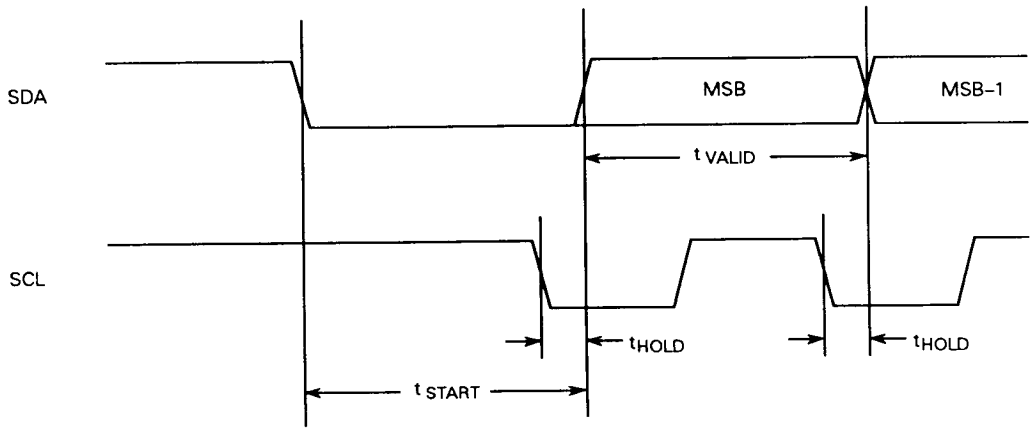
$t_{HOLD}$ = 1 Bus Cycle Time + $t_{pd}$          ($t_{pd} \approx 0 \rightarrow 30$ ns)

$t_{START} = t_{VALID}$ = 1 / I$^2$C Transfer Frequency    (I$^2$C Transfer Frequency determined by BD0/BD1)

**Figure 9-5. I$^2$C-bus Timing Diagram**