



# Am27C256

## 256 Kilobit (32,768 x 8-Bit) CMOS EPROM

### DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - 55 ns
- **Low power consumption**
  - 20  $\mu$ A typical CMOS standby current
- **JEDEC-approved pinout**
- **Single +5 V power supply**
- **$\pm 10\%$  power supply tolerance available**
- **100% Flashrite programming**
  - Typical programming time of 4 seconds
- **Latch-up protected to 100 mA from  $-1$  V to  $V_{CC} + 1$  V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - Both CMOS and TTL input/output compatibility
  - Two line control functions
- **Standard 28-pin DIP, PDIP, 32-pin TSOP and PLCC packages**

### GENERAL DESCRIPTION

The Am27C256 is a 256K-bit ultraviolet erasable programmable read-only memory. It is organized as 32K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP packages as well as plastic one time programmable (OTP) PDIP, TSOP, and PLCC packages.

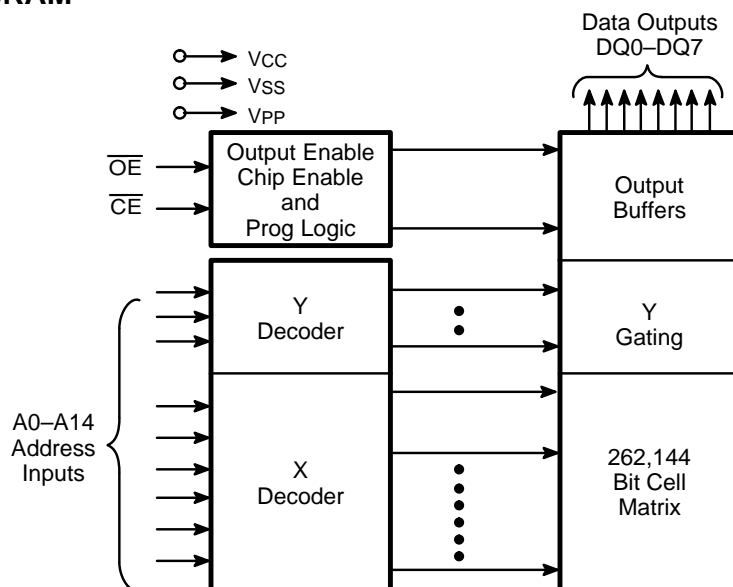
Typically, any byte can be accessed in less than 55 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C256 offers separate Output Enable ( $\overline{OE}$ ) and Chip Enable ( $\overline{CE}$ )

controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 80 mW in active mode, and 100  $\mu$ W in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C256 supports AMD's Flashrite programming algorithm (100  $\mu$ s pulses) resulting in typical programming time of 4 seconds.

### BLOCK DIAGRAM



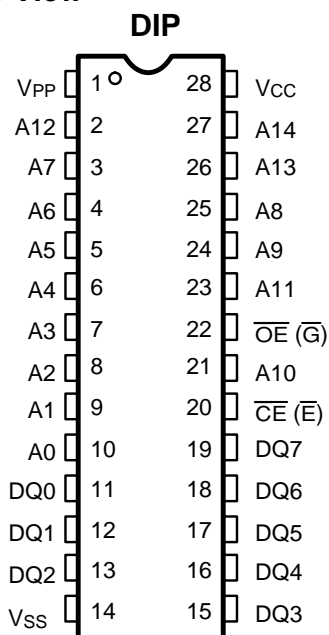
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## PRODUCT SELECTOR GUIDE

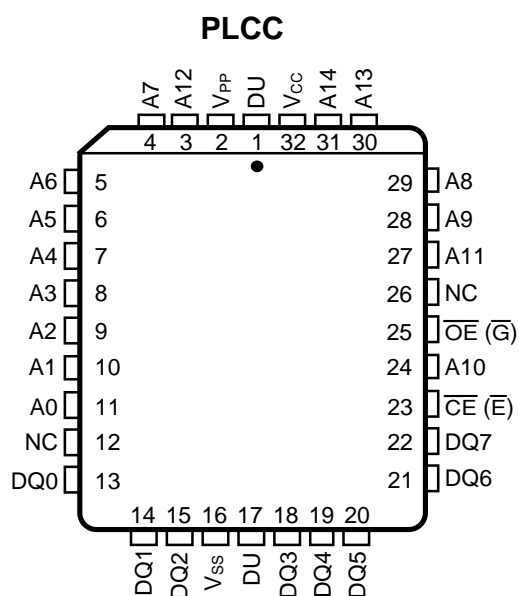
Family Part No.	Am27C256						
Ordering Part No: V <sub>CC</sub> ± 5%							-255
	-55	-70	-90	-120	-150	-200	
V <sub>CC</sub> ± 10%							
Max Access Time (ns)	55	70	90	120	150	200	250
$\overline{CE}$ ( $\overline{E}$ ) Access Time (ns)	55	70	90	120	150	200	250
$\overline{OE}$ ( $\overline{G}$ ) Access Time (ns)	35	40	40	50	50	50	50

## CONNECTION DIAGRAMS

### Top View



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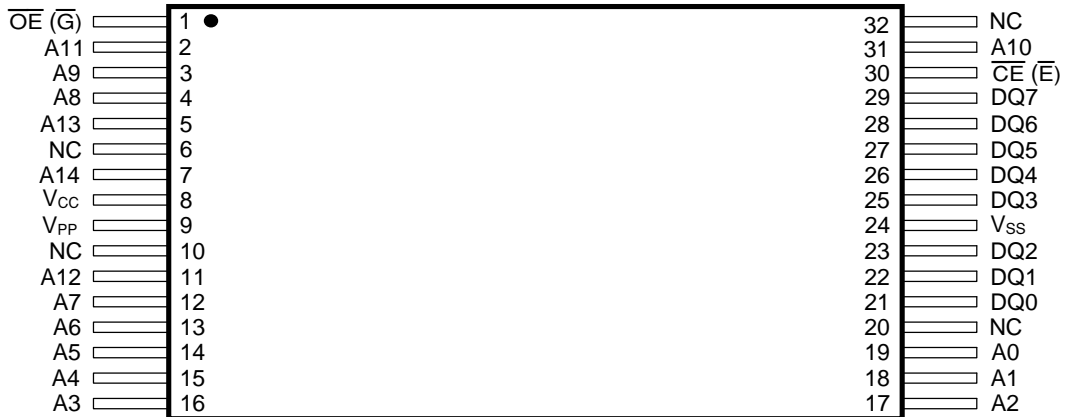
08007H-3

### Notes:

1. JEDEC nomenclature is in parentheses.

# CONNECTION DIAGRAM

TSOP\*



\*Contact local AMD sales office for package availability

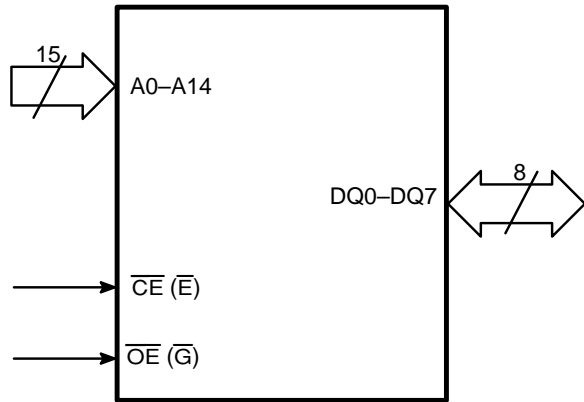
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## Standard Pinout

### PIN DESIGNATIONS

- A0–A14 = Address Inputs
- $\overline{CE} (\overline{E})$  = Chip Enable
- DQ0–DQ7 = Data Inputs/Outputs
- $\overline{OE} (\overline{G})$  = Output Enable Input
- V<sub>CC</sub> = V<sub>CC</sub> Supply Voltage
- V<sub>PP</sub> = Program Voltage Input
- V<sub>SS</sub> = Ground
- DU = Don't Use

### LOGIC SYMBOL

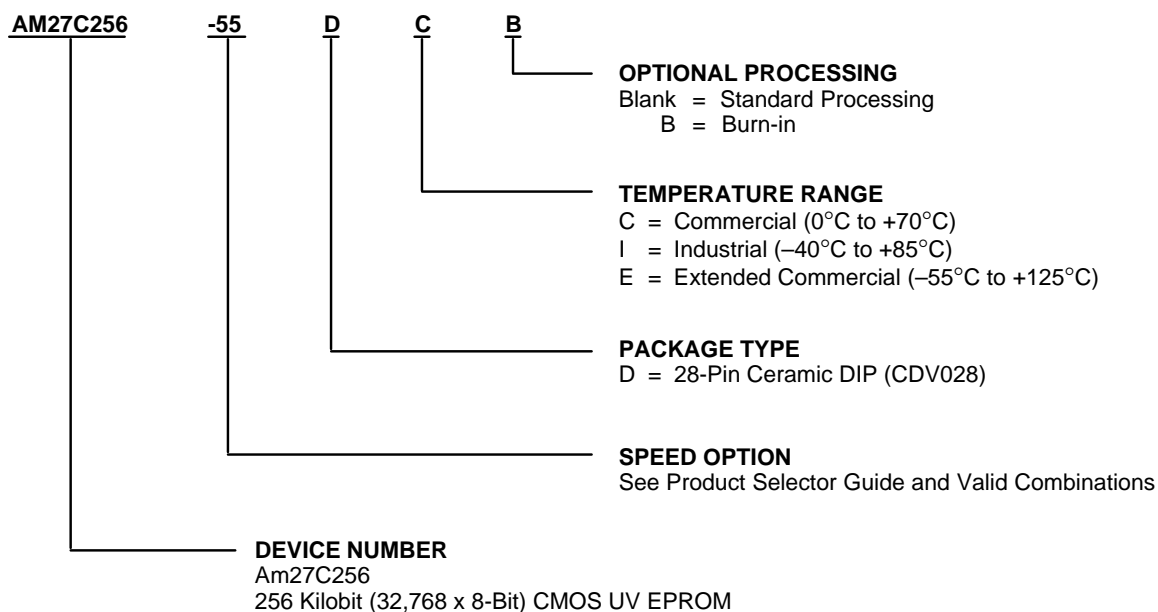


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## ORDERING INFORMATION

### UV EPROM Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C256-55	DC, DCB, DI, DIB
AM27C256-70	DC, DCB, DI, DIB, DE, DEB
AM27C256-90	
AM27C256-120	
AM27C256-150	
AM27C256-200	
AM27C256-255	DC, DCB, DI, DIB

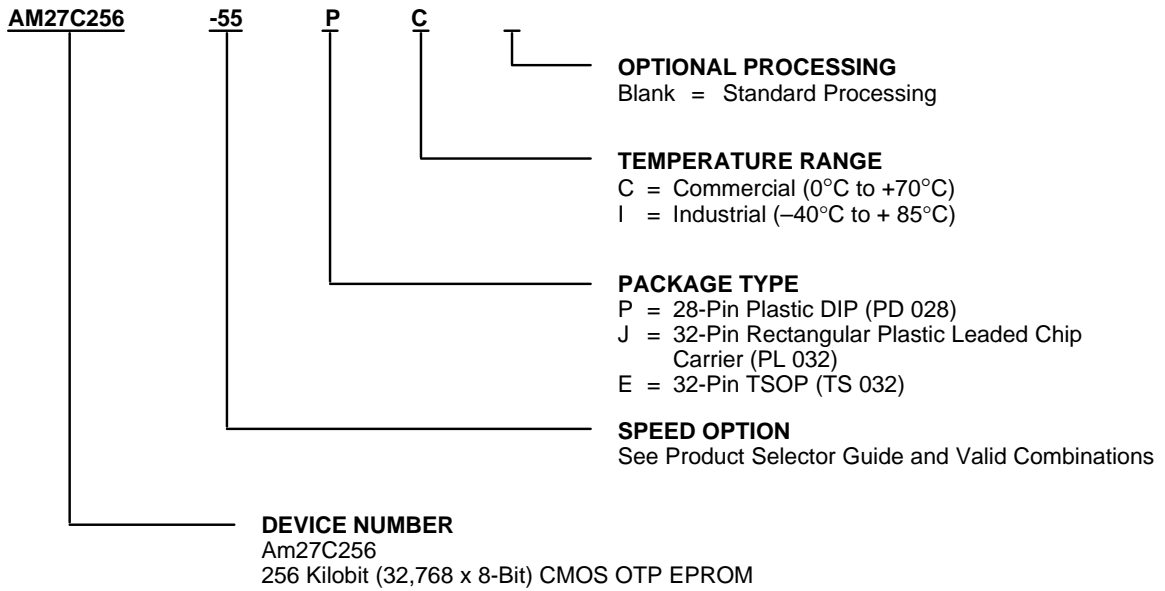
#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## ORDERING INFORMATION

### OTP Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C256-55	JC, PC, EC
AM27C256-70	JC, PC, EC, JI, PI, EI
AM27C256-90	
AM27C256-120	
AM27C256-150	
AM27C256-200	
AM27C256-255	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## FUNCTIONAL DESCRIPTION

### Erasing the Am27C256

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C256 to an ultraviolet light source. A dosage of 15 W sec/cm<sup>2</sup> is required to completely erase an Am27C256. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000 μW/cm<sup>2</sup> for 15 to 20 minutes. The Am27C256 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C256 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27C256 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

### Programming the Am27C256

Upon delivery or after each erasure the Am27C256 has all 262,144 bits in the “ONE” or HIGH state. “ZEROS” are loaded into the Am27C256 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V<sub>PP</sub> pin,  $\overline{OE}$  is at V<sub>IH</sub>, and  $\overline{CE}$  is at V<sub>IL</sub>.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 μs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C256. This part of the algorithm is done at V<sub>CC</sub> = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at V<sub>CC</sub> = V<sub>PP</sub> = 5.25 V.

Please refer to Section 6 for programming flow chart and characteristics.

### Program Inhibit

Programming of multiple Am27C256 in parallel with different data is also easily accomplished. Except for  $\overline{CE}$ , all like inputs of the parallel Am27C256 may be common. A TTL low-level program pulse applied to an Am27C256  $\overline{CE}$  input with V<sub>PP</sub> = 12.75 V ± 0.25 V, and

$\overline{OE}$  High will program that Am27C256. A high-level  $\overline{CE}$  input inhibits the other Am27C256 devices from being programmed.

### Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with  $\overline{OE}$  at V<sub>IL</sub>,  $\overline{CE}$  at V<sub>IH</sub>, and V<sub>PP</sub> between 12.5 V to 13.0 V.

### Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C256.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address like A9 of the Am27C256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V<sub>IL</sub> to V<sub>IH</sub>. All other address lines must be held at V<sub>IL</sub> during auto select mode.

Byte 0 (A0 = V<sub>IL</sub>) represents the manufacturer code, and byte 1 (A0 = V<sub>IH</sub>), the device code. For the Am27C256, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

### Read Mode

The Am27C256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t<sub>ACC</sub>) is equal to the delay from  $\overline{CE}$  to output (t<sub>CE</sub>). Data is available at the outputs t<sub>OE</sub> after the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been LOW and addresses have been stable for at least t<sub>ACC</sub>–t<sub>OE</sub>.

### Standby Mode

The Am27C256 has a CMOS standby mode which reduces the maximum V<sub>CC</sub> current to 100 μA. It is placed in CMOS-standby when  $\overline{CE}$  is at V<sub>CC</sub> ± 0.3 V. The Am27C256 also has a TTL-standby mode which reduces the maximum V<sub>CC</sub> current to 1.0 mA. It is placed in TTL-standby when  $\overline{CE}$  is at V<sub>IH</sub>. When in standby mode, the outputs are in a high-impedance state, independent of the  $\overline{OE}$  input.

## Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that  $\overline{CE}$  be decoded and used as the primary device-selecting function, while  $\overline{OE}$  be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

## System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1- $\mu$ F ceramic capacitor (high frequency, low inherent inductance) should be used on each device between  $V_{CC}$  and  $V_{SS}$  to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7- $\mu$ F bulk electrolytic capacitor should be used between  $V_{CC}$  and  $V_{SS}$  for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

## MODE SELECT TABLE

Mode		Pins	$\overline{CE}$	$\overline{OE}$	A0	A9	$V_{PP}$	Outputs
Read			$V_{IL}$	$V_{IL}$	X	X	X	DOUT
Output Disable			X	$V_{IH}$	X	X	X	High-Z
Standby (TTL)			$V_{IH}$	X	X	X	X	High-Z
Standby (CMOS)			$V_{CC} \pm 0.3 V$	X	X	X	X	High-Z
Program			$V_{IL}$	$V_{IH}$	X	X	$V_{PP}$	DIN
Program Verify			$V_{IH}$	$V_{IL}$	X	X	$V_{PP}$	DOUT
Program Inhibit			$V_{IH}$	$V_{IH}$	X	X	$V_{PP}$	High-Z
Auto Select (Note 3)	Manufacturer Code		$V_{IL}$	$V_{IL}$	$V_{IL}$	$V_{H}$	X	01H
	Device Code		$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{H}$	X	10H

### Notes:

1.  $V_H = 12.0 V \pm 0.5 V$
2. X = Either  $V_{IH}$  or  $V_{IL}$
3. A1–A8 = A10–A14 =  $V_{IL}$
4. See DC Programming Characteristics for  $V_{PP}$  voltage during programming.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
OTP Products	–65°C to +125°C
All Other Products	–65°C to +150°C
Ambient Temperature	
with Power Applied	–55°C to +125°C
Voltage with Respect To $V_{SS}$	
All pins except A9, $V_{PP}$ , $V_{CC}$	
(Note 1)	–0.6 V to $V_{CC} + 0.5$ V
A9 and $V_{PP}$ (Note 2)	–0.6 V to +13.5 V
$V_{CC}$	–0.6 V to +7.0 V

### Notes:

1. Minimum DC voltage on input or I/O pins is –0.5 V. During transitions, the inputs may overshoot  $V_{SS}$  to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is  $V_{CC} + 0.5$  V which may overshoot to  $V_{CC} + 2.0$  V for periods up to 20 ns.
2. For A9 and  $V_{PP}$  the minimum DC input is –0.5 V. During transitions, A9 and  $V_{PP}$  may overshoot  $V_{SS}$  to –2.0 V for periods of up to 20 ns. A9 and  $V_{PP}$  must not exceed 13.5 V for any period of time.

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ( $T_A$ ) . . . . . 0°C to +70°C

### Industrial (I) Devices

Ambient Temperature ( $T_A$ ) . . . . . –40°C to +85°C

### Extended Commercial (E) Devices

Ambient Temperature ( $T_A$ ) . . . . . –55°C to +125°C

### Supply Read Voltages

$V_{CC}$  for Am27C256-XX5 . . . . . +4.75 V to +5.25 V

$V_{CC}$  for Am27C256-XX0 . . . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

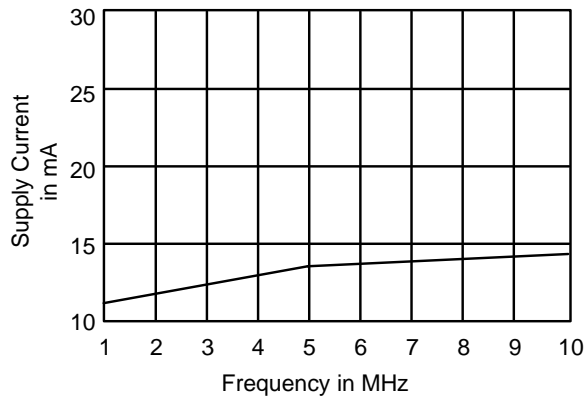


**DC CHARACTERISTICS over operating range unless otherwise specified.  
(Notes 1, 2 and 4)**

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -400 μA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA		0.45	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage		-0.5	+0.8	V
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0 V to +V <sub>CC</sub>		1.0	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0 V to +V <sub>CC</sub>	C/I Devices	1.0	μA
			E Devices	5.0	
I <sub>CC1</sub>	V <sub>CC</sub> Active Current (Note 3)	$\overline{CE} = V_{IL}$ , f = 10 MHz, I <sub>OUT</sub> = 0 mA		25	mA
I <sub>CC2</sub>	V <sub>CC</sub> TTL Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I <sub>CC3</sub>	V <sub>CC</sub> CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3 V$		100	μA
I <sub>PP1</sub>	V <sub>PP</sub> Current During Read	$\overline{CE} = \overline{OE} = V_{IL}$ , V <sub>PP</sub> = V <sub>CC</sub>		100	μA

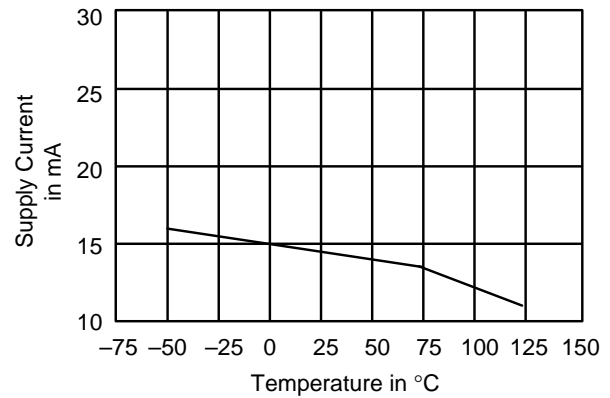
**Notes:**

- V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, and removed simultaneously or after V<sub>PP</sub>.
- Caution:** The Am27C256 must not be removed from (or inserted into) a socket when V<sub>CC</sub> or V<sub>PP</sub> is applied.
- I<sub>CC1</sub> is tested with  $\overline{OE} = V_{IH}$  to simulate open outputs.
- Minimum DC Input Voltage is -0.5 V. During transitions, the inputs may overshoot to -2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V<sub>CC</sub> + 0.5 V, which may overshoot to V<sub>CC</sub> + 2.0 V for periods less than 20 ns.



**Figure 1. Typical Supply Current vs. Frequency**  
V<sub>CC</sub> = 5.5 V, T = 25°C

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**Figure 2. Typical Supply Current vs. Temperature**  
V<sub>CC</sub> = 5.5 V, f = 10 MHz

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**CAPACITANCE**

Parameter Symbol	Parameter Description	Test Conditions	CDV028		PL 032		PD 028		TS 032		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0	8	12	8	12	6	10	10	12	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0	8	12	8	12	8	10	12	14	pF

**Notes:**

1. This parameter is only sampled and not 100% tested.
2. T<sub>A</sub> = +25°C, f = 1 MHz.

**SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4)**

Parameter Symbols		Parameter Description	Test Conditions	Am27C256							Unit	
JEDEC	Standard			-55	-70	-90	-120	-150	-200	-255		
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min	–	–	–	–	–	–	–	
				Max	55	70	90	120	150	200	250	ns
t <sub>ELQV</sub>	t <sub>CE</sub>	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min	–	–	–	–	–	–	–	
				Max	55	70	90	120	150	200	250	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min	–	–	–	–	–	–	–	
				Max	35	40	40	50	50	50	50	ns
t <sub>EHQZ</sub> , t <sub>GHQZ</sub>	t <sub>DF</sub> (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	–	–	–	–	–	–	–	
				Max	25	25	25	30	30	30	30	ns
t <sub>AXQX</sub>	t <sub>OH</sub>	Output Hold from Addresses, $\overline{CE}$ , or $\overline{OE}$ , whichever occurred first		Min	0	0	0	0	0	0	0	
				Max	–	–	–	–	–	–	–	ns

**Notes:**

1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, and removed simultaneously or after V<sub>PP</sub>.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27C256 must not be removed from (or inserted into) a socket or board when V<sub>PP</sub> or V<sub>CC</sub> is applied.
4. For the -55 and -70:

Output Load: 1 TTL gate and C<sub>L</sub> = 30 pF

Input Rise and Fall Times: 20 ns

Input Pulse Levels: 0 V to 3 V

Timing Measurement Reference Level: 1.5 V for inputs and outputs

For all other versions:

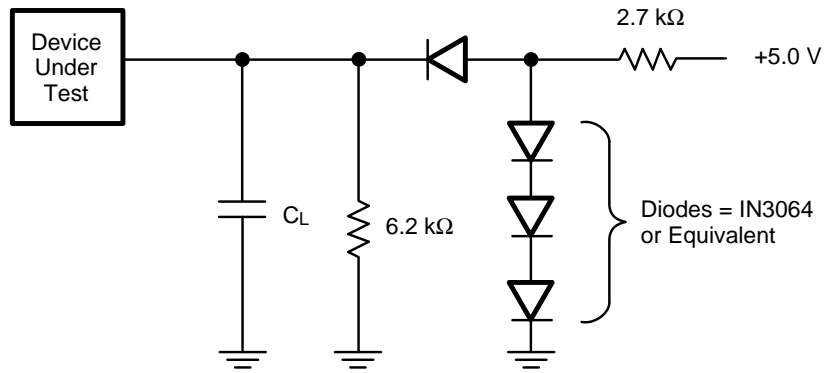
Output Load: 1 TTL gate and C<sub>L</sub> = 100 pF

Input Rise and Fall Times: 20 ns

Input Pulse Levels: 0.45 V to 2.4 V

Timing Measurement Reference Level: 0.8 V and 2 V inputs and outputs

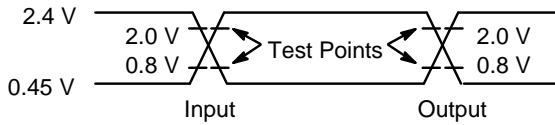
**SWITCHING TEST CIRCUIT**



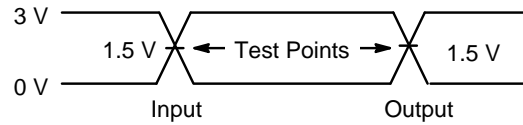
$C_L = 100 \text{ pF}$  including jig capacitance (30 pF for -55, -70)

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**SWITCHING TEST WAVEFORM**



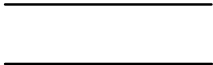
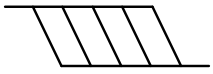

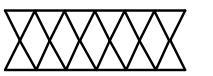
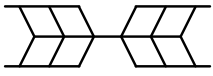
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are  $\leq 20 \text{ ns}$ .



AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are  $\leq 20 \text{ ns}$  for -55 and -70.

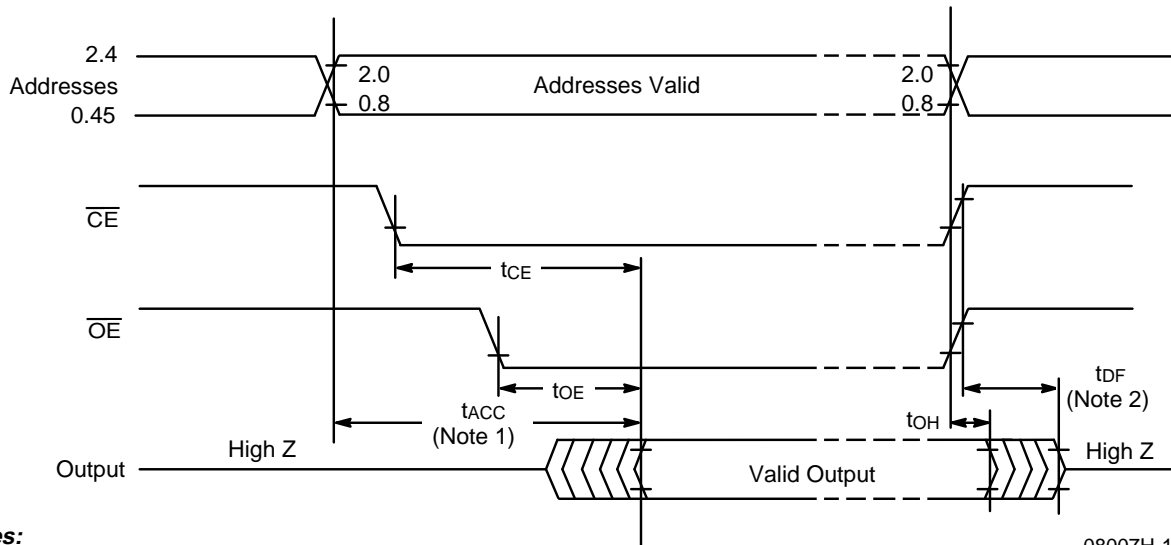
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## KEY TO SWITCHING TEST WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

KS000010

## SWITCHING WAVEFORMS



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**Notes:**

- $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the falling edge of the addresses without impact on  $t_{ACC}$ .
- $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.

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