

Data Sheet July 1999 File Number 2319.4

16A, 400V, 0.300 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17434.

Ordering Information

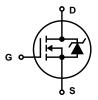
PART NUMBER	PACKAGE	BRAND
IRFP350	TO-247	IRFP350

NOTE: When ordering, include the entire part number.

Features

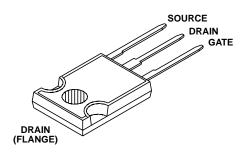
- 16A, 400V
- $r_{DS(ON)} = 0.300\Omega$
- Single Pulse Avalanche Energy Rated
- · SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- · Linear Transfer Characteristics
- · High Input Impedance
- · Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC STYLE TO-247 TOP VIEW



IRFP350

Absolute Maximum Ratings $T_C = 25^{\circ}C$, Unless Otherwise Specified

	IRFP350	UNITS
Drain to Source Voltage (Note 1)V _{DS}	400	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	400	V
Continuous Drain Current	16	Α
$T_C = 100^{\circ}C$ I_D	10	Α
Pulsed Drain Current (Note 3)	64	Α
Gate to Source Voltage	±20	V
Maximum Power Dissipation	180	W
Linear Derating Factor	1.44	W/oC
Single Pulse Avalanche Energy Rating (Note 4)	700	mJ
Operating and Storage Temperature	-55 to 150	°С
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	300	οС
Package Body for 10s, See Techbrief 334	260	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}C$ to $125^{\circ}C$.

Electrical Specifications $T_C = 25^{\circ}C$, Unless Otherwise Specified

Drain to Source Breakdown Voltage BVDSS VGS = 0V, ID = 250μA VGS = 50μA Gate to Threshold Voltage VGS(TH) VGS = VDS, ID = 250μA Zero-Gate Voltage Drain Current IDSS VDS = Rated BVDSS, VGS = 0V VDS = 0.8 x Rated BVDSS, VGS = 0V, TJ = 125°C VDS = 0.8 x Rated BVDSS, VGS = 0V, TJ = 125°C On-State Drain Current (Note 2) ID(ON) VDS > ID(ON) x PDS(ON)MAX. VGS = 10V (Figure 7) Gate to Source Leakage Current IGSS VGS = ±20V Drain to Source On Resistance (Note 2) rDS(ON) VGS = 10V, ID = 8.9A (Figures 8, 9) Forward Transconductance (Note 2) gfs VDS = 2 x VGS, ID = 8.0A (Figures 8, 9) Forward Transconductance (Note 2) gfs VDS = 2 x VGS, ID = 8.0A (Figures 8, 9) Forward Transconductance (Note 2) gfs VDS = 2 x VGS, ID = 8.0A (Figures 8, 9) Forward Transconductance (Note 2) gfs VDD = 200V, ID = 16A, RGS = 6.2Ω, VGS = 10V, RE = 12.3C MOSFET Switching Times are Essentially Independent of Operating Temperature MCSFET Switching Times are Essentially Independent of Operating Temperature Gate to Source Hoater (Gate to Drain) Qg VGS = 10V, ID = 16A, VDS = 0.8 x Rated BVDSS. IG(REF) = 1.5mA (Figure 14) State Charge is Essentially Independent of Operatin	MIN	ΛIN	TYP	MAX	UNITS
	400	100	-	-	V
$V_{DS} = 0.8 \times Rated BV_{DSS}, V_{GS} = 0V, T_{J} = 125^{\circ}C$ On-State Drain Current (Note 2) $I_{D(ON)} V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, V_{GS} = 10V (Figure 7)$ Gate to Source Leakage Current $I_{GSS} V_{GS} = \pm 20V$ Drain to Source On Resistance (Note 2) $I_{DS}(ON) V_{GS} = 10V, I_{D} = 8.9A (Figure 8.9)$ Forward Transconductance (Note 2) $I_{TURO}(ON) V_{DS} = 22 \times V_{GS}, I_{D} = 8.0A (Figure 12)$ $I_{TURO}(ON) V_{DS} = 200V, I_{D} = 16A, R_{GS} = 6.2\Omega, V_{GS} = 10V, R_{L} = 12.3\Omega$ $I_{TURO}(OF) I_{TURO}(OF) I_{TURO}(OF$	2.0	2.0	-	4.0	V
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	-	-	-	25	μΑ
Gate to Source Leakage Current IGSS VGS = ±20V Drain to Source On Resistance (Note 2) rDS(ON) VGS = 10V, ID = 8.9A (Figures 8, 9) Forward Transconductance (Note 2) gfs VDS = 2 x VGS, ID = 8.0A (Figure 12) Turn-On Delay Time tD(ON) VDD = 200V, ID = 16A, RGS = 6.2Ω, VGS = 10V, RE = 12.3Ω MOSFET Switching Times are Essentially Independent of Operating Temperature Temperature Fall Time tf VGS = 10V, ID = 16A, VDS = 0.8 x Rated BVDSS, IG(REF) = 1.5mA (Figure 14) Gate to Source + Gate to Drain) Qg VGS = 10V, ID = 16A, VDS = 0.8 x Rated BVDSS, IG(REF) = 1.5mA (Figure 14) Gate to Source Charge Qgs Temperature Gate to Drain "Miller" Charge Qgd Input Capacitance CISS VGS = 0V, VDS = 25V, f = 1.0MHz (Figure 11) Output Capacitance CRSS Reverse-Transfer Capacitance CRSS Internal Drain Inductance LD Measured Between the Contact Screw on Header that is Closer to Source and Gate Pins and Center of Die Modified MOSFET Symbol Showing the Internal Devices Inductances Internal Source Inductance LS Measured from the Source Lead, 6mm (0.25in) From Header to	-	-	-	250	μΑ
$ \begin{array}{ c c c c c } \hline Drain to Source On Resistance (Note 2) & r_{DS(ON)} & V_{GS} = 10V, I_D = 8.9A \ (Figures 8, 9) \\ \hline Forward Transconductance (Note 2) & g_{fs} & V_{DS} = 2 \times V_{GS}, I_D = 8.0A \ (Figure 12) \\ \hline Turn-On Delay Time & t_{D(ON)} & V_{DD} = 200V, I_D = 16A, R_{GS} = 6.2\Omega, V_{GS} = 10V, \\ R_{LS} = 12.3\Omega & MOSFET Switching Times are Essentially \\ Turn-Off Delay Time & t_{f} & MOSFET Switching Times are Essentially Independent of Operating Temperature \\ \hline Fall Time & t_{f} & & & & & & & & & \\ Total Gate Charge & Q_{g} & V_{GS} = 10V, I_D = 16A, V_{DS} = 0.8 \times Rated BV_{DSS}. \\ I_{G(REF)} = 1.5mA \ (Figure 14) & Gate Charge is Essentially Independent of Operating Temperature \\ \hline Gate to Drain "Miller" Charge & Q_{gd} & Gate Charge is Essentially Independent of Operating Temperature \\ \hline Gate to Drain "Miller" Charge & Q_{gd} & Gate Charge is Essentially Independent of Operating Temperature \\ \hline U_{DUTU} Capacitance & C_{ISS} & V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz \ (Figure 11) & & & & & & & & & \\ \hline U_{DUTU} Capacitance & C_{RSS} & & & & & & & & & \\ \hline Internal Drain Inductance & L_D & Measured Between the Contact Screw on Header that is Closer to Source and Gate Pins and Center of Die & Gource Lead, 6mm (0.25in) From Header to & Gource Lead, $	16	16	-	-	Α
Forward Transconductance (Note 2) gfs VDS = 2 x VGS, ID = 8.0A (Figure 12) Turn-On Delay Time tD(ON) VDD = 200V, ID = 16A, RGS = 6.2Ω, VGS = 10V, RL = 12.3Ω Rise Time tr RL = 12.3Ω Turn-Off Delay Time tD(OFF) Fall Time tf Total Gate Charge (Gate to Source + Gate to Drain) Qg VGS = 10V, ID = 16A, VDS = 0.8 x Rated BVDSS. IG(REF) = 1.5mA (Figure 14) Gate to Source Charge Qgs Gate Charge is Essentially Independent of Operating Temperature Gate to Drain "Miller" Charge Qgd Input Capacitance CISS VGS = 0V, VDS = 25V, f = 1.0MHz (Figure 11) Output Capacitance CRSS Internal Drain Inductance LD Measured Between the Contact Screw on Header that is Closer to Source and Gate Pins and Center of Die Modified MOSFET Symbol Showing the Internal Devices Inductances Induc	-	-	-	±100	nA
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	-	- (0.250	0.300	Ω
Rise Time tr RL = 12.3Ω Turn-Off Delay Time tD(OFF) Fall Time tf Total Gate Charge (Gate to Source + Gate to Drain) Qg V _{GS} = 10V, I _D = 16A, V _{DS} = 0.8 x Rated BV _{DSS} . I _{G(REF)} = 1.5mA (Figure 14) Gate to Source Charge Qgs Gate Charge is Essentially Independent of Operating Temperature Gate to Drain "Miller" Charge Qgd Input Capacitance CISS Reverse-Transfer Capacitance CRSS Internal Drain Inductance LD Measured Between the Contact Screw on Header that is Closer to Source and Gate Pins and Center of Die Modified MOSFET Symbol Showing the Internal Devices Inductances Internal Source Inductance LS Measured from the Source Lead, 6mm (0.25in) From Header to	8.0	8.0	10	-	S
Turn-Off Delay Time Torn-Off Delay Time to Double to Double to Source Gate to Drain to Source Gate Charge is Essentially Independent of Operating Temperature	-	-	12	18	ns
Turn-Off Delay Time Fall Time Total Gate Charge (Gate to Source + Gate to Drain) Gate to Source Charge Gate to Drain "Miller" Charge Qgd Input Capacitance Coss Reverse-Transfer Capacitance Cnss Internal Drain Inductance Ls Measured from the Source Lead, 6mm (0.25in) From Header to Inductance Coss Internal Source Inductance Inductance Ls Measured Source (Coss Inductance (Coss Inductance (Coss Inductance (Coss Inductance (Coss Internal Drain Inductance (Coss Inductance (C	-	-	51	77	ns
Total Gate Charge (Gate to Source + Gate to Drain) Gate to Source Charge Gate to Drain "Miller" Charge Input Capacitance Clss Reverse-Transfer Capacitance Internal Drain Inductance Internal Source Inductance Ls Measured Between the Contact Screw on Header that is Closer to Source and Gate Pins and Center of Die Measured From Header to Source Inductance Ls Measured from the Source Lead, 6mm (0.25in) From Header to	-	-	75	110	ns
Gate to Source + Gate to Drain Gate to Source Charge Qgs	-	-	47	71	ns
Gate to Drain "Miller" Charge Input Capacitance	-	-	87	130	nC
Gate to Drain "Miller" Charge Qgd	-	-	10	-	nC
Output Capacitance Coss Reverse-Transfer Capacitance CRSS Internal Drain Inductance LD Measured Between the Contact Screw on Header that is Closer to Source and Gate Pins and Center of Die Internal Source Inductance LS Measured Form the Source Lead, 6mm (0.25in) From Header to	-	-	33	-	nC
Reverse-Transfer Capacitance CRSS Internal Drain Inductance LD Measured Between the Contact Screw on Header that is Closer to Source and Gate Pins and Center of Die Internal Source Inductance LS Measured Form the Source Lead, 6mm (0.25in) From Header to	-	-	2000	-	pF
Internal Drain Inductance LD Measured Between the Contact Screw on Header that is Closer to Source and Gate Pins and Center of Die Internal Source Inductance LS Measured Between the Contact Screw on Header Symbol Showing the Internal Devices Inductances Modified MOSFET Symbol Showing the Internal Devices Inductances Symbol Showing the Internal Devices Inductances Measured Between the Contact Screw on Header Symbol Showing the Internal Devices Inductances On Device Inductance Inductance LS Measured Between the Contact Screw on Header Symbol Showing the Internal Devices Inductances On Device Inductance Inducta	-	-	400	-	pF
Contact Screw on Header that is Closer to Source and Gate Pins and Center of Die Internal Source Inductance Ls Measured from the Source Lead, 6mm (0.25in) From Header to	-	-	100	•	pF
Source Lead, 6mm (0.25in) From Header to	-	-	5.0	-	nH
ds	-	-	12.5	-	nH
Junction to Case R _{θJC}	-	-	-	0.70	°C/W
Junction to Ambient R _{0JA} Free Air Operation	-	-	-	30	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I _{SD}	Modified MOSFET	Q D	-	-	16	Α
Pulse Source to Drain Current (Note 3)	I _{SDM}	Symbol Showing the Integral Reverse P-N Junction Diode	G S S	-	-	64	A
Source to Drain Diode Voltage (Note 2)	V _{SD}	$T_J = 25^{\circ}C$, $I_{SD} = 16A$, $V_{GS} = 0V$ (Figure 13)		i	-	1.6	V
Reverse Recovery Time	t _{rr}	$T_J = 150^{o}C$, $I_{SD} = 15A$, $dI_{SD}/dt = 100A/\mu s$		270	-	1300	ns
Reverse Recovered Charge	Q _{RR}	$T_J = 150^{\circ}C$, $I_{SD} = 15A$, $dI_{SD}/dt = 100A/\mu s$		1.7	-	8.1	μC

NOTES:

- 2. Pulse Test: Pulse width $\leq 300 \mu s$, duty cycle $\leq 2\%$.
- 3. Repetitive Rating: Pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
- 4. V_{DD} = 40V, starting T_J = 25°C, L = 5.66mH, R_G = 50 Ω , peak I_{AS} = 15A.

Typical Performance Curves Unless Otherwise Specified

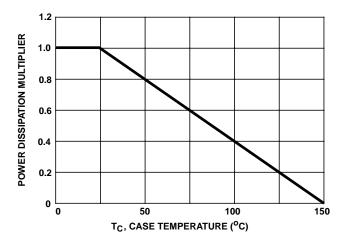


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

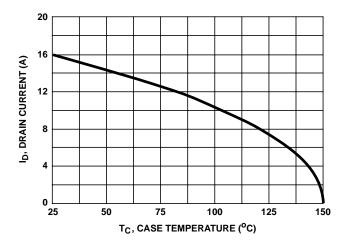


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

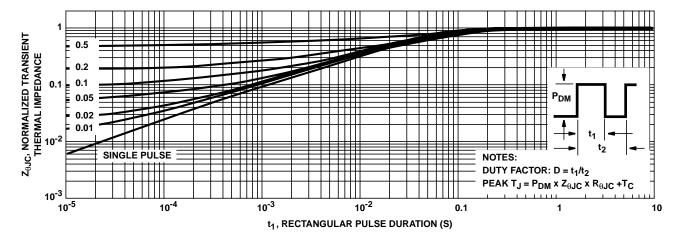


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified (Continued)

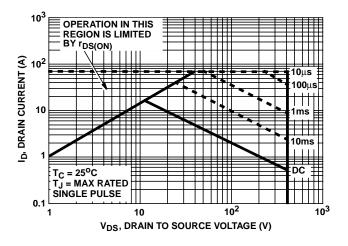


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

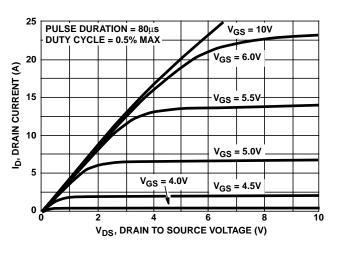


FIGURE 6. SATURATION CHARACTERISTICS

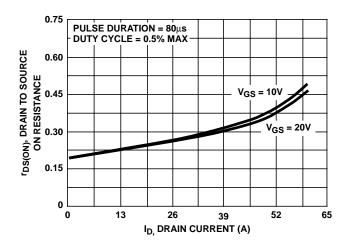


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

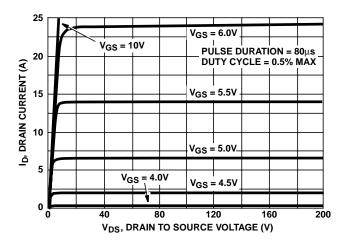


FIGURE 5. OUTPUT CHARACTERISTICS

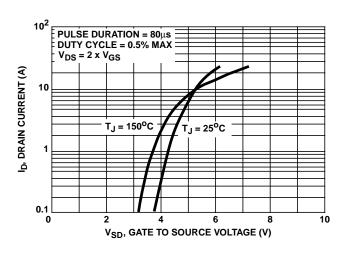


FIGURE 7. TRANSFER CHARACTERISTICS

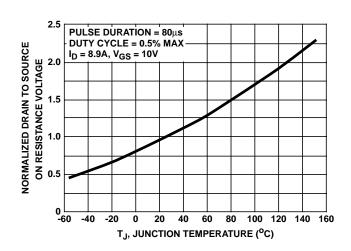


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

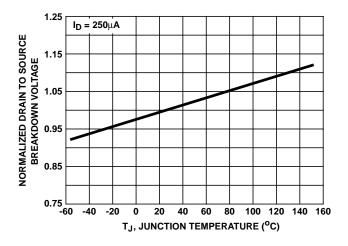


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

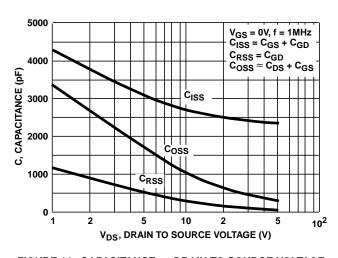


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

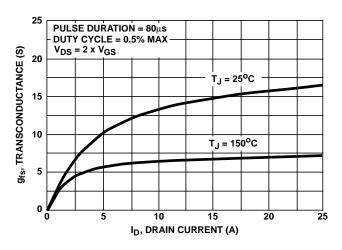


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

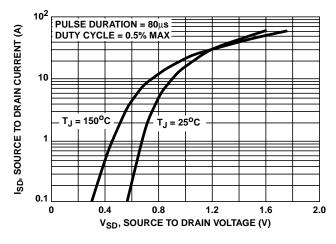


FIGURE 13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

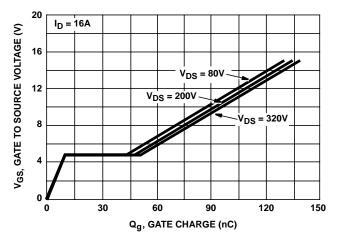


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

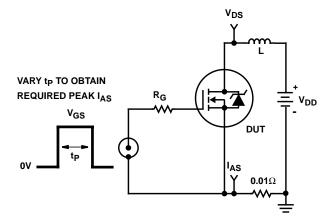


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

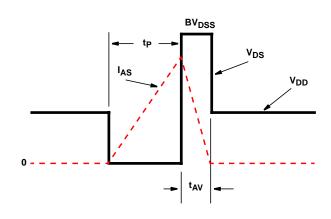


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

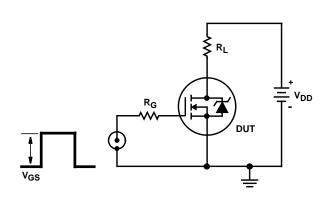


FIGURE 17. SWITCHING TIME TEST CIRCUIT

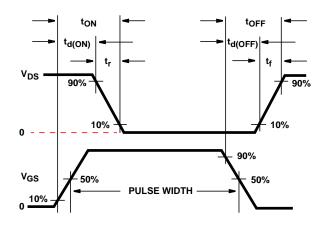


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

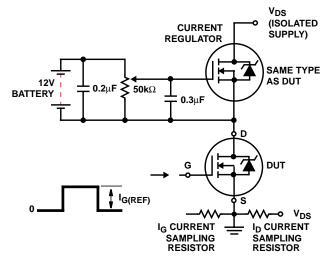


FIGURE 19. GATE CHARGE TEST CIRCUIT

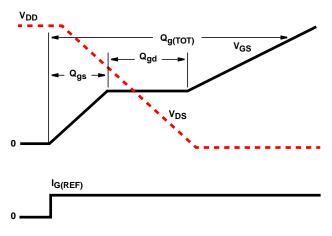


FIGURE 20. GATE CHARGE WAVEFORMS

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