THOMSON COMPONENTS
MOSTEK

TS27C64P-15/20/25/30

65.536-BIT (8192 x 8) CMOS ONE TIME PROGRAMMABLE-ROM

MEMORY COMPONENTS

ADVANCE INFORMATION

The TS27C64P is a high speed 64K bits one time electrically programmable ROM ideally suited for applications where fast turn-around is an important requirement.

The TS27C64P is packaged in a 28-pin dual-in-line plastic package and therefore can not be re-written. Programming is performed according to standard THOMSON SEMICONDUCTEURS 64K EPROM procedure.

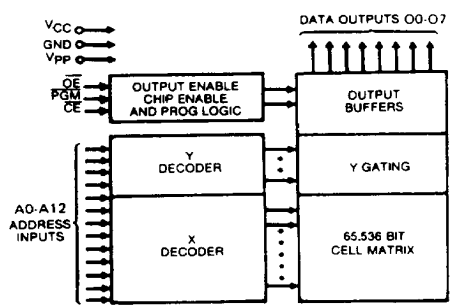
- Compatible to standard TS27C64 (electrical parameters)
- Programming voltage 12.5 V
- High speed programming
- 28-pin JEDEC approved pin-out
- Ideal for automatic insertion
- Also proposed in PLCC (32 pins JEDEC standard)

TABLE 1: ORDERING INFORMATION

PART NUMBER	t_{ACC} (ns)	t_{CE} (ns)	t_{OE} (ns)	V_{CC}
TS27C64P-15	150	150	75	5V ± 10%
TS27C64P-20	200	200	80	5V ± 10%
TS27C64P-25	250	250	100	5V ± 10%
TS27C64P-30	300	300	120	5V ± 10%

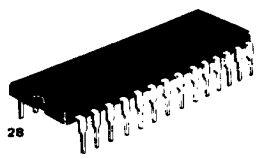
Operating temperature range
0°C to+ 70°C (CP suffix), – 40°C to+ 85°C (VP suffix)
– 40°C to 105°C (TP suffix)

BLOCK DIAGRAM



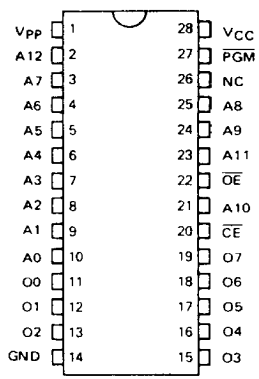
CMOS

65.536-BIT
(8192 x 8)
ONE TIME PROGRAMMABLE-ROM



P SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENT



PIN NAMES

A0-A12	Address
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0-O7	Outputs
$\overline{PGM}$	Program
NC	Non Connected

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Operating temperature range TS27C64CP TS27C64VP TS27C64TP	T_{amb}	T_L to T_H 0 to+ 70 − 40 to+ 85 − 40 to+ 105	°C
Storage temperature range	T_{stg}	−65 to + 125	°C
Supply voltage	V_{PP}*	−0.6 to + 14	V
Input voltage A9 Except V_{PP}, A9	V_{in}*	−0.6 to + 13.5 −0.6 to + 6.25	V
Max power dissipation	P_D	1.5	W
Lead temperature (Soldering : 10 seconds)		+ 300	°C

* With respect to V_{SS}

Note 1 : "Maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating temperature range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical characteristics" provides conditions for actual device operation.

READ OPERATION (Note 2)

DC CHARACTERISTICS

$T_{amb} = T_L$ to T_H, $V_{CC} = 5$ V ± 10 %, $V_{SS} = 0$ V (Unless otherwise specified)

Characteristic	Symbol	Min	Typ (Note 2)	Max	Unit
Input load current (V_{in}= V_{CC} or GND)	I_{LI}	–	–	10	µA
Ouput leakage current (V_{out}= V_{CC} or V_{SS}, $\overline{CE}$ = V_{IH})	I_{LO}	–	–	10	µA
V_{PP} read voltage	V_{PP}	V_{CC} −0.7	–	V_{CC}	V
Input low voltage	V_{IL}	−0.1	–	0.8	V
Input high voltage (Note 2)	V_{IH}	2.0	–	V_{CC}+ 1	V
Output low voltage I_{OL}= 2.1 mA I_{OL}= 0 µA	V_{OL}	– –	– –	0.45 0.1	V
Output high voltage I_{OH}= −400 µA I_{OH}= 0 µA	V_{OH}	2.4 V_{CC} − 0.1	– –	– –	V
V_{CC} supply active current (TTL levels) $\overline{CE}$ = $\overline{OE}$ = V_{IL}, Inputs= V_{IH} or V_{IL}, f= 5 MHz, I/O= 0 mA	I_{CC2}	–	10	30	mA
V_{CC} supply standby current $\overline{CE}$ = V_{IH} $\overline{CE}$ = V_{CC}	I_{CCSB1} I_{CCSB2}	– –	0.5 10	1 100	mA µA
V_{PP} read current (V_{PP}= V_{CC}= 5.5 V)	I_{PP1}	–	–	100	µA

AC CHARACTERISTICS (Notes 3, 4, 5)

$T_{amb} = T_L$ to T_H

Characteristic	Symbol	Min	Maximum values				Unit
			TS27C64 -15	TS27C64 -20	TS27C64 -25	TS27C64 -30	
Address to output delay ($\overline{CE}$ = $\overline{OE}$ = V_{IL})	t_{ACC}	–	150	200	250	300	ns
CE to output delay ($\overline{OE}$ = V_{IL})	t_{CE}	–	150	200	250	300	ns
Output enable to output delay ($\overline{CE}$ = V_{IL})	t_{OE}	–	75	80	100	120	ns
Output enable high to output float ($\overline{CE}$ = V_{IL})	t_{DF} (Note 4)	0	50	50	60	105	ns
Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occured first ($\overline{CE}$ = $\overline{OE}$ = V_{IL})	t_{OH}	0	–	–	–	–	ns

CAPACITANCE (Note 5)
T_{amb} = + 25° C, f = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input capacitance (V_{in} = 0V)	C_{in}	–	4	6	pF
Output capacitance (V_{out} = 0 V)	C_{out}	–	8	12	pF

Note 2 : Typical conditions are for operation at : T_{amb} = + 25°C, V_{CC} = 5 V, V_{PP} = V_{CC}, and V_{SS} = 0 V

Note 3 : V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}
V_{PP} may be connected to V_{CC} except during program.

Note 4 : The t_{DF} compare level is determined as follows :
High to THREE-STATE, the measured V_{OH}(DC) – 0.1V
Low to THREE-STATE the measured V_{OL}(DC) + 0.1V.

Note 5: Capacitance is guaranteed by periodic testing. T_{amb} = + 25° C, f = 1 MHz

AC TEST CONDITIONS (Figure 1,2)

Output Load	1 TTL Gate and C_L = 100 pF
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs , Outputs	0.8V and 2V

FIGURE 1 – OUTPUT LOAD CIRCUIT

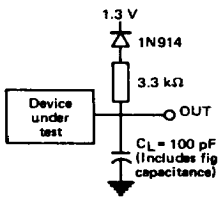
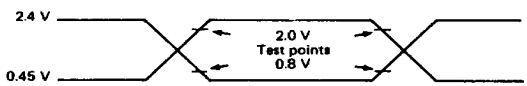
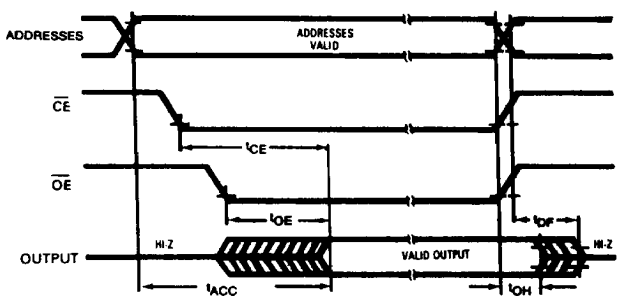


FIGURE 2 – AC TESTING INPUT/OUTPUT WAVEFORM



AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8V for a logic "0".

AC WAVEFORMS (READ MODE)



DC PROGRAMMING CHARACTERISTICS

T_{amb} = 25 ± 5°C, V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V (Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Input current (all inputs - $V_I = V_{IL}$ or V_{IH})	I_I	–	–	10	μA
Input low level (all inputs)	V_{IL}	-0.1	–	0.8	V
Input high level	V_{IH}	2.0	–	V_{CC} + 1	V
Output low voltage during verify (I_{OL} = 2.1 mA)	V_{OL}	–	–	0.45	V
Output high voltage during verify (I_{OH} = - 400 μA)	V_{OH}	2.4	–	–	V
V_{CC} supply current (Program & Verify)	I_{CC3}	–	–	30	mA
V_{PP} supply current (Program - $\overline{CE} = V_{IL} = \overline{PGM}$)	I_{PP2}	–	–	30	mA

AC PROGRAMMING CHARACTERISTICS

T_{amb} = 25 ± 5°C, V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V (Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Address set-up time	t_{AS}	2	–	–	μs
$\overline{OE}$ set-up time	t_{OES}	2	–	–	μs
Data set-up time	t_{DS}	2	–	–	μs
Address hold time	t_{AH}	0	–	–	μs
Data hold time	t_{DH}	2	–	–	μs
Output enable to output float delay	t_{DF}	0	–	130	ns
V_{PP} set-up time	t_{VPS}	2	–	–	μs
V_{CC} set-up time	t_{VCS}	2	–	–	μs
$\overline{PGM}$ initial program pulse width	t_{PW}	0.95	1.0	1.05	ms
$\overline{PGM}$ overprogram pulse width (Note 2)	t_{OPW}	2.85	–	78.75	ms
$\overline{CE}$ set-up time	t_{CES}	2	–	–	μs
Data valid from $\overline{OE}$	t_{OE}	–	–	150	ns

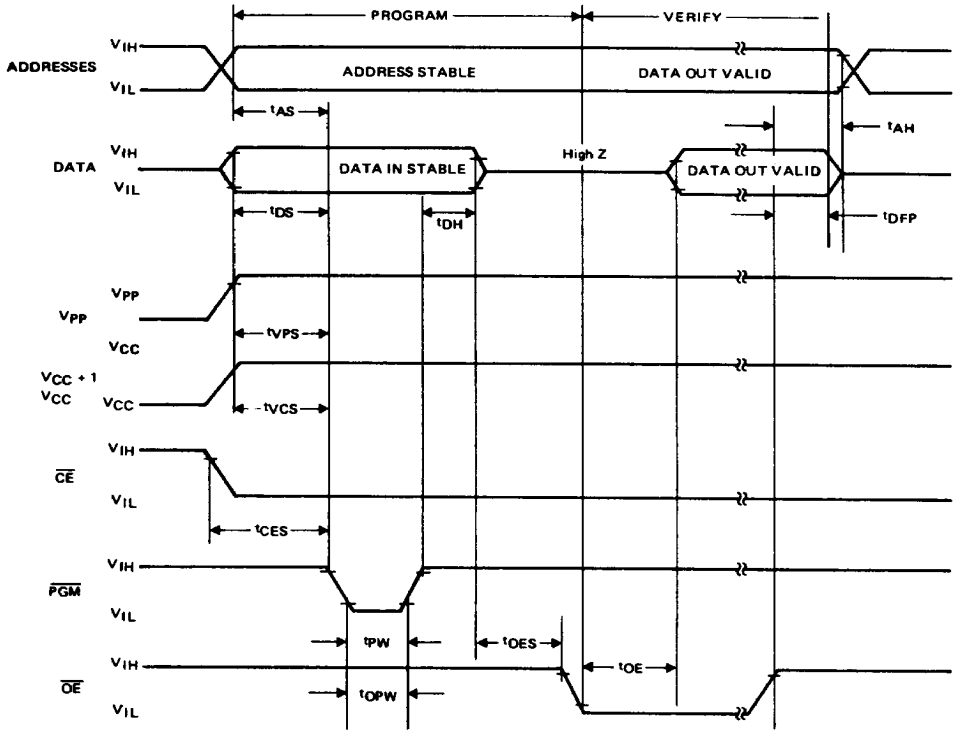
AC TEST CONDITIONS

Input rise and fall times (10% to 90%)	20ns
Input pulse levels	0.45V to 2.4V
Input timing reference level	0.8V and 2.0V
Ouptut timing reference level	0.8V and 2.0V

Note 1 : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 2 : t_{OPW} is defined in flow chart.

HIGH SPEED PROGRAMMING WAVE FORMS



1. The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the TS27C64, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

TABLE 2. MODE SELECTION

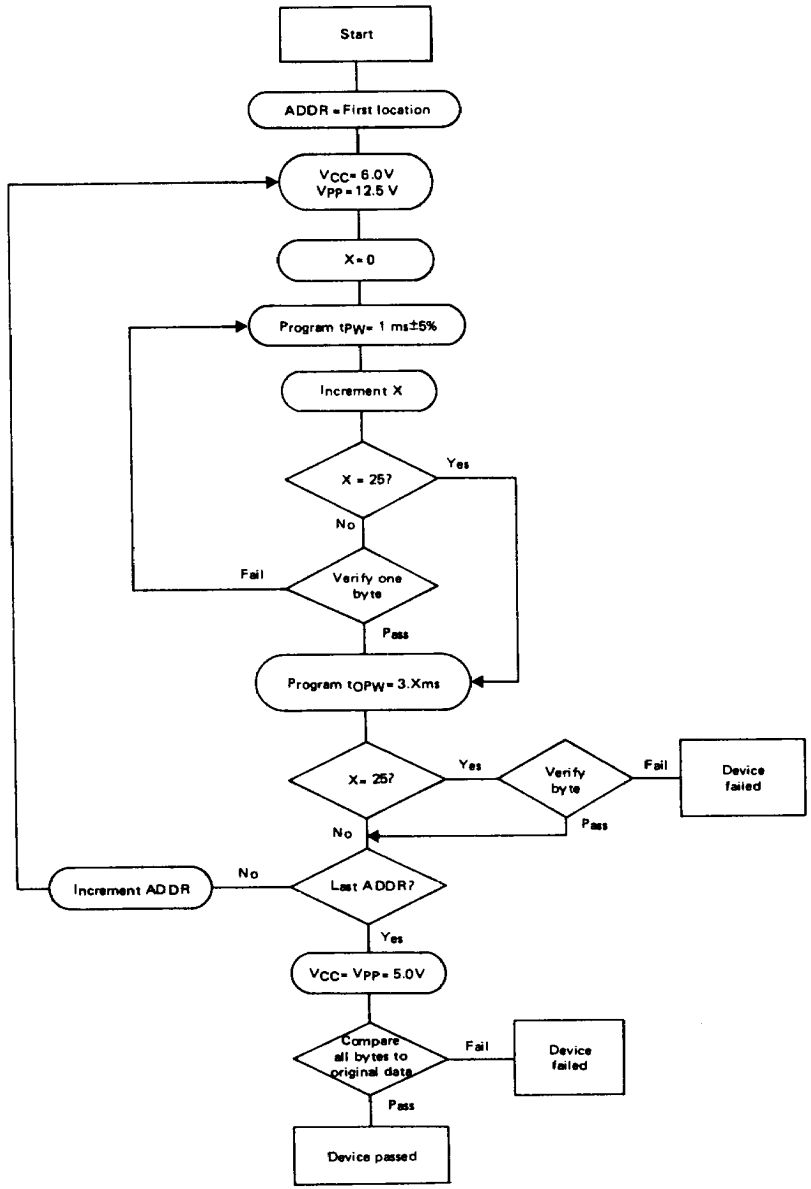
Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13 15-19)
Read	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	V_{CC}	Hi-Z
High speed programming	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	Hi-Z
Electronic signature (Note 3)	V_{IL}	V_{IL}	V_H Note 2	V_{IH}	V_{CC}	V_{CC}	CODE

NOTES : 1 - X can be either V_{IL} or V_{IH}

2 - V_H = 12.0 V ± 0.5 V

3 - All address lines at V_{IL} except A9 and A0 that is toggled from V_{IL} (manufacturer code: 98) to V_{IH} (type code: 08).

HIGH SPEED PROGRAMMING FLOW CHART



FUNCTIONAL DESCRIPTION

DEVICE OPERATION

The seven modes of operation of the TS27C64 are listed in Table 2. A single 5V power supply is required in the read mode. All inputs are TTL levels except for Vpp.

Read Mode

The TS27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of $t_{\overline{OE}}$ from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-$t_{\overline{OE}}$.

Standby Mode

The TS27C64 has a standby mode which reduces the maximum power dissipation to 5.5 mW. The TS27C64 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMs are usually used in larger memory arrays, we have provided two control lines which accommodate this multiple memory connection. The two control lines allow for :

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To use these control lines most efficiently, $\overline{CE}$ (pin 20) should be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming modes

CAUTION : Exceeding 14V on pin 1(Vpp) will damage the TS27C64.

Initially, and after each erasure, all bits of the TS27C64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The TS27C64 is in the programming mode when the Vpp input is at 12.5 V and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. It is required that a 0.1 μF capacitor be placed across Vpp, V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Programming of multiple TS27C64s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel TS27C64s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled TS27C64s.

- **High speed programming**

  The high speed programming algorithm described in the flow chart page 6 rapidly programs TS27C64 using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of 1 minute.

- **Program inhibit**

  Programming of multiple TS27C64s in parallel with different data is also easily accomplished by using the program inhibit mode. A high level on $\overline{CE}$ or $\overline{PGM}$ inputs inhibits the other TS27C64s from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel TS27C64s may be common. A TTL low-level pulse applied to a TS27C64 $\overline{CE}$ and $\overline{PGM}$ inputs with Vpp at 12.5 V will program that TS27C64.

- **Program verify**

  A verify may be performed on the programmed bits to determine that they were correctly programmed. The verify is performed with $\overline{CE}$ and $\overline{OE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and Vpp at 12.5 V.

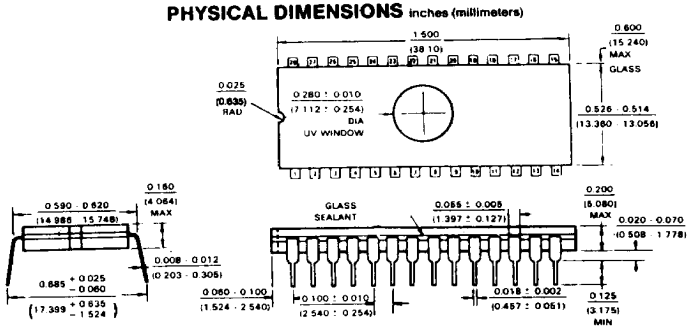
- **Electronic signature mode**

  Electronic signature mode allows the reading out of a binary code that will identify the EPROM manufacturer and type.

  This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the TS27C64.

  To activate this mode the programming equipment must force 11.5 V to 12.5 V on address line A9 (pin 24) of the TS27C64. Two bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during electronic signature mode.

PHYSICAL DIMENSIONS inches (millimeters)



These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.