MC68605

Technical Summary

X.25 Protocol Controller

The MC68605 X.25 protocol controller (XPC) is an intelligent HCMOS communications protocol controller that implements the 1984 International Telegraph and Telephone Consultative Committee (CCITT) X.25 Recommendation data link access procedure (LAPB). It supports full-duplex point-to-point serial communication at up to 10 Mbps and relieves the host processor of managing the communications link by providing sequencing using HDLC framing, error control, retransmission based upon a cyclic redundancy check (CRC), and flow control using the receive-not-ready supervisory frame. The XPC directly supports the physical level interfaces (Recommendation X.21 physical level, X.21 *bis*, and V-series) and also provides an efficient interface to the packet level for information and control exchange. Key features of the XPC include:

- Fully Implements X.25 Recommendation LAPB Procedure by Independently Generating Link-Level Commands and Responses
- Option To Implement X.75 Recommendation
- Optional Transparent Operation (Monitor Mode) where XPC Provides High-Level/Synchronous Data Link Control (HDLC/SDLC) Framing Functions for User-Generated Frames
- Performs Direct Memory Access (DMA) Transfer of Information Frames to and from Memory Using Two On-Chip 22-Byte FIFOs
- Primary Communication through Shared Memory Structures with a Powerful Command Set to Off-Load Data Link Management
- Flexible Rx/Tx Linked Memory Structures Minimize Host Intervention and Simplify Memory Management
- Basic (Modulo 8) and Extended (Modulo 128) Operation
- Automatic Comparison of the Programmable Local and Remote Addresses
- Detects Programmable Time-Out and Retries Limit Conditions
- 16- or 32-Bit CRC Generation and Checking

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- Standard Modem Interface
- NRZ or NRZI Encoding/Decoding
- Vectored Interrupts and Status Reporting
- Built-In Diagnostics Provide Local Loopback and External Loopback Testing
- Up to 10-Mbps Synchronous Serial Data Rate
- 12.5- and 10-MHz System Clock Versions
- 8- and 16-Bit Data Bus Support
- 32-Bit Address Bus with Virtual Address Capability
- M68000 Family Asynchronous Bus Structure
- Programmable Byte Ordering of Data for Alternate Memory Organization Schemes

GENERAL DESCRIPTION

The XPC supports high-speed X.25 communications between host computers, between host computers and remote units, and between remote units. The XPC also supports a transparent operation mode that does not apply the LAPB procedure. Data is passed between the XPC and the host processor through shared memory structures, permitting a minimum command set for host processor/XPC communication. The XPC is also a full M68000 bus master, providing on-chip DMA capability for management of memory tables and frame buffers. Since the XPC data bus interface is configurable, the XPC can handle both 8- and 16-bit data transfers.

When the X.25 mode is selected by the user, the XPC is configured as a combined station for full-duplex point-to-point communication. The XPC supports a nonoperational mode and two operational modes as defined by the LAPB procedure. The nonoperational mode is asynchronous disconnect mode (ADM). In this balanced data link mode, the combined station is logically disconnected from the data link and is not permitted to transmit or accept information. Operational modes include asynchronous balanced mode (ABM) and asynchronous balanced mode extended (ABME). A balanced data link allows a combined station to send a command or initiate a response frame transmission without receiving explicit permission from the other station. In ABM/ABME, the XPC performs the following operations:

1. Transmission of a chain of information (I) frames when instructed by the host,

2. Transmission of supervisory (S) frames as defined by the X.25 LAPB Recommendation,
3. Transmission of unnumbered (U) commands as required or when instructed by the host, and
4. Transmission of unnumbered (U) responses as defined by the X.25 LAPB Recommendation.

When the transparent mode is selected, the XPC can be configured as a master, a slave, or a combined station for full-duplex operation. The XPC can support any HDLC/SDLC-defined operational mode (see Figure 1). All frames are user generated and are transmitted only when instructed by the host.

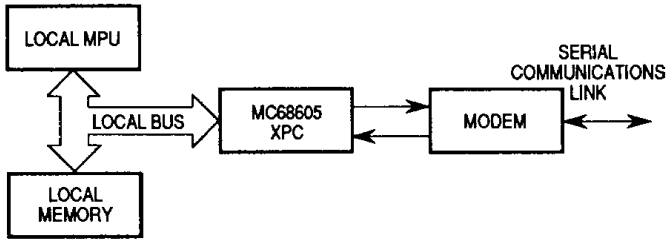

Figure 1. XPC System Configuration

INTERNAL REGISTERS

The XPC has four functional blocks: serial, DMA, microcode controller, and register file/arithmetic logic unit (ALU). Each section contains user-visible and nonvisible registers that define and control the operation of the XPC. A block diagram of the XPC is shown in Figure 2.

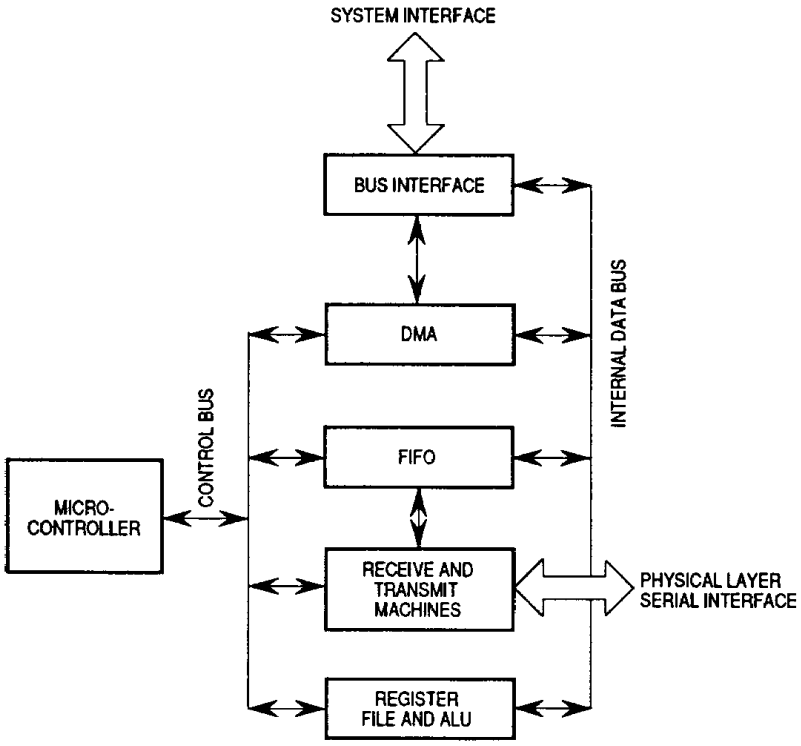

Figure 2. Block Diagram

Because the XPC communicates with the host primarily through shared memory, minimal host-processor-accessible registers are required. Registers in the XPC fall into two groups. One group is directly accessible by the user, and the other group is indirectly accessible through the station table. The directly accessible registers include the command register, semaphore register, interrupt vector register, and data register. The complete register set is shown in Table 1.

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Table 1. XPC Register Set

Directly Accessible Registers	
Register	**Description**
Command	8-Bit Write Only
Semaphore	8-Bit Read Only
Interrupt Vector	8-Bit Write Only, Read on Host Processor Interrupt Acknowledge Cycle
Data	32-Bit Write Only

Indirectly Accessible Registers	
Register	**Mnemonic**
Station Table Pointer	STP
Station Table Function Code	STFC
Local Address	LA
Remote Address	RA
Hardware Configuration	HC
Station Configuration	SC
Option Bits	OB
Mode Descriptor	MD
Frame Reject Descriptor	FRD
Rx/Host Status	RHS
Tx/Link Status	TLS

Register	Mnemonic
V(S)	V(S)
V(R)	V(R)
Time Scale Divider	TSD
Retries Count	RC
Transmit Table Pointer	TTP
Transmit Table Function Code	TTFC
Transmit Buffer Pointer	TBP
Transmit Buffer Function Code	TBFC
Transmit Buffer Count	TBC
Receive Table Pointer	RTP
Receive Table Function Code	RTFC
Receive Buffer Pointer	RBP
Receive Buffer Function Code	RBFC
Receive Buffer Count	RBC
Time-Out Preset	TOP
Retries Limit	RL
Outstanding Frames Limit	OFL
Pad Time Select	PTS
Last Received N(R)	LRN

SHARED MEMORY STRUCTURES

The host processor communicates with the XPC using three tables located in shared memory (see Figure 3). The station table allows the host processor to initialize and update the XPC operating parameters and table pointers and to receive status and error information. The transmit frame specification table queues frames to be transmitted by the XPC, and the receive frame specification table queues available receive buffers for the XPC to store received information frames. The XPC is given a pointer to the station table during initialization. The transmit frame specification table and receive frame specification table pointers are contained in the station table.

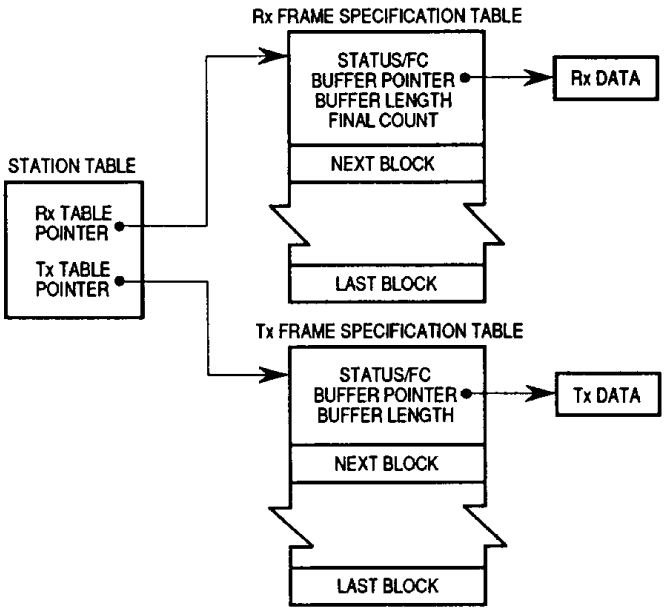

Figure 3. Shared Memory Tables

STATION TABLE

The station table format is shown in Figure 4. The first 19 words of the station table are written by the host processor and are read by the XPC. This portion of the table contains the XPC operating information. The XPC accesses this table area as the result of a host processor command. The next 22 words of the table are written by the XPC and read by the host processor. Some of these entries are written by the XPC as the result of a command while other entries are updated by the XPC when a change occurs. When the XPC accesses the table as the result of a host processor command, it sets the semaphore register to $FF upon completion of the last access. While the XPC is processing a command, the semaphore register is $FE.

WORD	15 12	11 8	7 4	3 0
0	OPTION BITS			
1	TIME-OUT PRESET			
2	TIME SCALE DIVIDER		PAD TIME SELECT	
3	OUTSTANDING FRAMES LIMIT		RETRIES LIMIT	
4	Rx/HOST MASK BITS			
5	Tx/LINK MASK BITS			
6	Rx/HOST STATUS CLEAR BITS			
7	Tx/LINK STATUS CLEAR BITS			
8	0 0 0 0	0 0 0 0	LOCAL ADDRESS	
9	0 0 0 0	0 0 0 0	REMOTE ADDRESS	
10	0 0 0 0	0 0 0 0	0 0 0 0	RTFC
11	RECEIVE TABLE POINTER — HIGH WORD			
12	RECEIVE TABLE POINTER — LOW WORD			
13	0 0 0 0	0 0 0 0	0 0 0 0	TTFC
14	TRANSMIT TABLE POINTER — HIGH WORD			
15	TRANSMIT TABLE POINTER — LOW WORD			
16	0 0 0 0	0 0 0 0	0 0 0 0	DAFC
17	DUMP AREA POINTER — HIGH WORD			
18	DUMP AREA POINTER — LOW WORD			

HOST PROCESSOR AREA: READ BY THE XPC; WRITTEN BY HOST PROCESSOR

19	Rx/HOST STATUS			
20	Tx/LINK STATUS			
21	MODE DESCRIPTOR		FRAME REJECT DESCRIPTOR	
22	V(S)		V(R)	
23	0 0 0 0	0 0 0 0	0 0 0 0	FUFC
24	FIRST UNACKNOWLEDGED POINTER — HIGH WORD			
25	FIRST UNACKNOWLEDGED POINTER — LOW WORD			
26	0 0 0 0	0 0 0 0	0 0 0 0	TFC
27	TRANSMIT POINTER — HIGH WORD			
28	TRANSMIT POINTER — LOW WORD			
29	0 0 0 0	0 0 0 0	0 0 0 0	RTFC
30	RECEIVE POINTER — HIGH WORD			
31	RECEIVE POINTER — LOW WORD			
32	0 0 0 0	0 0 0 0	0 0 0 0	REFC
33	RECEIVE BUS/ADDRESS ERROR POINTER — HIGH WORD			
34	RECEIVE BUS/ADDRESS ERROR POINTER — LOW WORD			
35	0 0 0 0	0 0 0 0	0 0 0 0	TEFC
36	TRANSMIT BUS/ADDRESS ERROR POINTER — HIGH WORD			
37	TRANSMIT BUS/ADDRESS ERROR POINTER — LOW WORD			
38	RECEIVED FRMR INFORMATION FIELD — WORD 1			
39	RECEIVED FRMR INFORMATION FIELD — WORD 2			
40	RECEIVED FRMR INFORMATION FIELD — WORD 3			

XPC AREA: READ BY THE HOST PROCESSOR; WRITTEN BY THE XPC

Figure 4. Station Table Structure

TRANSMIT FRAME SPECIFICATION TABLE

The transmit frame specification table queues transmit frames for the XPC. These frames are stored in memory buffers located throughout memory. The transmit frame specification table contains a sequential list of transmit frame specification blocks. The transmit frame specification blocks describe the location of transmit buffers and provide information about the transmit queue. The transmit table pointer location in the station table points to the first transmit frame specification block (see Figure 5).

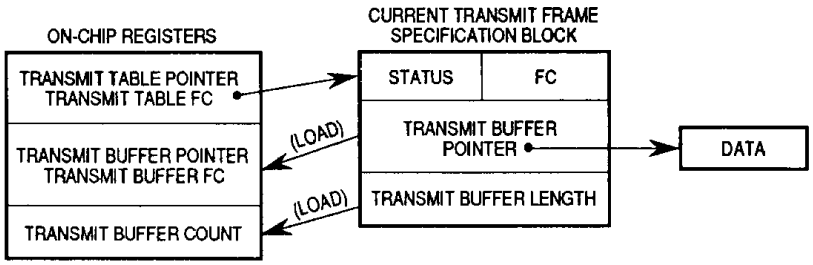

Figure 5. Transmit Frame Specification Table

When the host processor instructs the XPC to load transmit table pointer, the XPC loads the transmit table pointer and transmit table function code registers from the corresponding station table entries. The transmit table pointer register then has the address of the first transmit frame specification block. Before the transmission of each frame, the XPC accesses the current transmit frame specification block to load the transmit buffer function code, transmit buffer address, and transmit buffer length into the corresponding internal registers. The XPC presents a transmit buffer address and function code to the system to load the information contained in the transmit buffer.

During transparent operation, the XPC accesses the next transmit frame specification block and transmits the corresponding frame buffer until the end of the transmit frame specification table is reached. The XPC updates its internal V(S) register after the transmission of each frame. When all frames have been transmitted, the XPC sets the information frames acknowledged (IFAK) bit in the Tx/link status register.

During X.25 operation, the XPC accesses the next transmit frame specification block and transmits the corresponding frame buffer according to the X.25 Recommendation until reaching either the outstanding frames limit or the end of the transmit frame specification table. The XPC updates its internal V(S) registers after the transmission of an information frame. The XPC monitors the N(R) of incoming frames until all transmitted frames have been acknowledged.

After all frames have been acknowledged, the XPC sets the IFAK bit in the Tx/link status register.

RECEIVE FRAME SPECIFICATION TABLE

The receive frame specification table queues receive buffers for the XPC. These buffers are stored throughout memory. The receive frame specification table contains a sequential list of receive frame specification blocks. The receive frame specification blocks describe the location of the receive buffers and provide information about the queue. The receive table pointer in the station table points to the first receive frame specification block (see Figure 6).

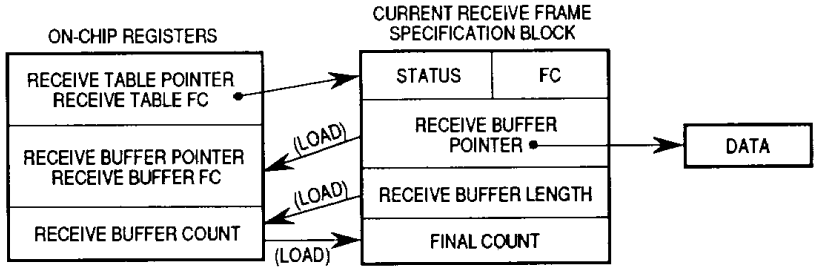

Figure 6. Receive Frame Specification Table

When the host processor instructs the XPC to load receive table pointer, the XPC loads the receive table function code and receive table pointer registers from the corresponding station table entries. The receive table pointer register then contains the address of the first receive frame specification block. The XPC accesses the receive frame specification block to load the receive buffer function code, receive buffer address, and the receive buffer length into its internal registers. The XPC then presents the receive buffer address and function code to the system to store the received information field in the memory buffer. After reception of a frame, the XPC writes the number of unused bytes in the final count entry in the current receive frame specification block and updates its internal V(R) register. Next, the XPC sets the receive information frame (RXI) bit in the Rx/host status register. The XPC accesses the next receive frame specification block to store incoming frames until reaching the end of the receive frame specification table.

To decrease the possibility of a receive-not-ready condition due to a lack of available receive buffers, a method is provided for linking receive frame specification tables. When the end of table (EOT) bit is set in a receive frame specification block, the XPC inspects the link bit value. If the link bit is set, then the XPC loads the receive table pointer and function code registers from the cor-

responding station table locations. The XPC then sets the receive table ended (RTE) bit in the Rx/host status register and issues an interrupt if enabled. The link operation can be used to implement a cyclical queue by using the original receive table pointer and function code values in the station table. However, the user must read filled receive buffers expediently to ensure that the XPC does not overwrite the buffers with incoming frames.

COMMAND SET

The host processor issues commands to the XPC to perform various functions by writing to the XPC command register. There are 23 commands that fall in the following four categories:

1. Initialization
2. Table Handling
3. Link Handling
4. Test/Diagnostics

INITIALIZATION COMMANDS

Initialization commands configure the XPC for operation after a hardware or software reset. The four initialization commands specify various system attributes, communication protocol options, and the location of the station table in memory.

Reset

The RESET command and hardware reset causes the following actions:

- Reset the Receive Channel and Isolate RxD
- Reset the Transmit Channel, Negate $\overline{\text{RTS}}$, and Transmit Ones
- Immediately Relinquish the System Bus
- Set the Interrupt Vector Register to $0F
- Disable Transmit and Receive Memory Buffers
- Clear All Rx/Host and Tx/Link Status Bits
- Clear All Hardware and Station Configuration Bits
- Clear All Option Bits
- Clear All Mode Descriptor and Frame Reject Descriptor Bits
- Zero Station Table Pointer and Station Table Function Code Registers
- Zero Transmit Table Pointer and Transmit Table Function Code Registers
- Zero Receive Table Pointer and Receive Table Function Code Registers
- Zero Remote Address and Local Address Registers
- Zero V(R), V(S), and Last Received N(R) Registers
- Zero Preset Values and Retries Count Register

Set Station Configuration

The SET STATION CONFIGURATION command specifies protocol parameters. The command has the following format:

7	6	5	4	3	2	1	0
1	0	1	0	ECRC	0	ECNT	0

ECRC — Extended CRC
- 0 = 16-Bit CRC
  CRC CCITT ($X^{16}+X^{12}+X^5+1$)
- 1 = 32-Bit CRC
  ($X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+11$
  $+X^{10}+X^8+X^7+X^5+X^4+X^2+X^1+1$)

ECNT — Extended Control
- 0 = Basic Control Field Format (Modulo 8)
- 1 = Extended Control Field Format (Modulo 128)

Set Hardware Configuration

The SET HARDWARE CONFIGURATION command defines the data decoding/encoding scheme, DMA burst control, data organization in memory, and data bus size. The format of the command is as follows:

7	6	5	4	3	2	1	0
1	1	0	NRZI	BRSC	0	DORGM	BUSW

NRZI — Non-Return to Zero Invert
- 0 = NRZ Decoding/Encoding
- 1 = NRZI Decoding/Encoding

BRSC — Burst Control
- 0 = DMA Burst is Unlimited
- 1 = DMA Burst is Limited to Eight Successive Memory Cycles

DORGM — Data Organization in Memory for a 16-Bit Data Bus System
- 0 = Data in Memory is Organized with High-Order Byte in Lower Memory Address (Motorola and IBM™ Convention)
- 1 = Data in Memory is Organized with Low-Order Byte in Lower Memory Address (DEC™ and Intel™ Convention)
  (This capability is available only for I-frame buffers and not for parameters or tables.)

BUSW — Bus Width
0 = 8-Bit Data Bus
1 = 16-Bit Data Bus

Load Function Code

The LOAD FUNCTION CODE command writes the function code value in the data register into the station table function code register. This command is issued after the host processor has written the function code to the data register.

Load Station Table Pointer

The LOAD STATION TABLE POINTER command writes the station table address from the data register into the station table pointer register. This command is issued after the host processor has written the station table pointer to the data register.

TABLE HANDLING COMMANDS

The 11 table handling commands cause the XPC to access the station table, transmit frame specification table, or receive frame specification table.

Load Option Bits

The LOAD OPTION BITS command loads the option set from the station table into the option bits register.

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	X.75

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	CRCNOA

X.75 — X.75 Option
0 = X.25 Operation
1 = X.75 Operation

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Intel is a trademark of Intel Corporation.

CRCNOA — CRC Bypass Option
0 = Non-octet aligned frames or frames with a CRC error are not accepted.
1 = Non-octet aligned frames or frames with a CRC error are accepted.

Load Addresses

The LOAD ADDRESSES command loads the local and remote addresses from the station table into the internal XPC registers. After these registers are loaded, the XPC is ready to establish the link. The XPC monitors the receive line and transmits continuous flags.

Load Preset Values

The LOAD PRESET VALUES command loads the time-out preset value, time scale divider, pad time select, outstanding frames limit, and retries limit from the station table into the respective XPC internal registers.

Load Transmit Table Pointer

The LOAD TRANSMIT TABLE POINTER command loads the transmit table pointer and the transmit table function code from the station table into the corresponding XPC registers and enables the transmission of a chain of information frames.

Continue Transmit

The CONTINUE TRANSMIT command ($95) is used to extend the transmit queue after adding entries to the transmit frame specification table. The user should set EOT in the transmit status location of the last added entry and then clear EOT at the previous end of table. Finally, the user should issue the CONTINUE TRANSMIT command to the XPC. This command is useful in the case where the XPC has already detected the previous EOT and will not read a new table entry. Instead, it is waiting for all transmitted frames to be acknowledged; during this period, it will not accept a new load transmit table pointer command.

Load Receive Table Pointer

The LOAD RECEIVE TABLE POINTER command loads the receive table pointer and the receive table function code from the station table into the corresponding XPC registers and enables the reception of information frames.

Load Station Parameters

The LOAD STATION PARAMETERS command combines the load option bits, load preset values, and load addresses commands.

Update Status

The UPDATE STATUS command allows the host to request current XPC status information.

Clear Tx/Link Status

The CLEAR Tx/LINK STATUS command clears the status bits in the Tx/link status register as specified by the Tx/link status clear bits in the station table.

Clear Rx/Host Status

The CLEAR Rx/LINK STATUS command clears the Rx/host status register as specified by the Rx/host status clear bits in the station table.

Clear Status

The CLEAR STATUS command clears both the Tx/link and Rx/host status bits in the respective XPC registers as specified by the Tx/link status clear bits and the Rx/host status clear bits in the station table.

Dump Parameters

The DUMP PARAMETERS command writes the following XPC parameters into the corresponding status table locations in the order given: Rx/host status, Tx/link status, mode descriptor, frame reject descriptor, V(R), V(S), first unacknowledged transmit block function code and pointer, next transmit block function code and pointer, and next receive block function code and pointer.

LINK HANDLING COMMANDS

The two link handling commands cause the XPC to set the link to a new operation mode and to automatically handle communication on both channels according to the predefined configuration and option bits.

Start Link

The START LINK command initiates the link setup procedure.

Stop Link

The STOP LINK command initiates the link disconnect procedure.

TEST/DIAGNOSTICS

The five commands in the text/diagnostics category test the XPC circuit and run diagnostics on the link.

Dump Registers

The DUMP REGISTERS command writes the XPC registers to a user-specified dump area in external memory.

DMA Transfer

The DMA TRANSFER command tests the handling of parallel data. The XPC reads the data from a transmit memory buffer and writes it to a receive memory buffer. The XPC transfers data from the transmit buffer to the receive buffer via the data register without using the internal transmit or receive FIFOs. The serial link is not affected by this operation.

Serial Loopback

The SERIAL LOOPBACK command tests the handling of parallel and serial data. The XPC reads data from the transmit memory buffer into the transmit FIFO. The data is then serialized and shifted internally into the receive FIFO and onto the TxD line. Finally, the data is stored in the receive memory buffer. $\overline{RTS}$ is not active during serial loopback.

Monitor

The MONITOR COMMAND allows the XPC to check the communication channel by reading/writing the entire frame from/to memory. The monitor command may be used to perform an external loopback test of the system or to implement any HDLC/SDLC operation mode where all frames are user generated. The XPC transmits and/or receives multiple information frames using the transmit and receive frame specification tables until receiving an end monitor command.

The user places the address, control, and data (if any) fields in each transmit buffer. The XPC only provides framing, zero insertion, and CRC for each frame. On the receive side, the XPC strips off flags, handles zero deletion, and writes the address, control and data fields into the receive buffer. The received CRC is also appended to the end of each memory buffer and is verified by the XPC.

End Monitor

The END MONITOR command terminates the monitor command.

XPC IMPLEMENTATION OF LAPB PROTOCOL

INITIALIZATION PROCEDURE

The XPC enters the initialization procedure as the result of a hardware or software reset. During this initialization, the station table address and function code, system configuration information, and XPC interrupt vector are loaded by the XPC under the direction of the host, as shown in the following sample program. Internal XPC registers directly accessed during the initialization procedure are the command register (CR), data register (DR), interrupt vector register (IV), and semaphore register (SR).

RESET

```
  Repeat: Read Semaphore Register Until It Is FF
Write CR: Set Hardware Configuration
  Repeat: Read Semaphore Register Until It Is FF
Write CR: Set Station Configuration
  Repeat: Read Semaphore Register Until It Is FF
Write DR: 4-Bit Function Code Value for Station Table Access
Write CR: Load Function Code
  Repeat: Read Semaphore Register Until It Is FF
Write DR: 32-Bit Address of Station Table
Write CR: Load Station Table Pointer
  Repeat: Read Semaphore Register Until It Is FF
 Write IV: Load Interrupt Vector
Write CR: Load Station Table Parameters
  Repeat: Read Semaphore Register Until It Is FF
```

NOTE

The XPC will not come out of hardware or software reset without the system clock and the transmit clock. The transmit clock is used to initialize the serial section of the chip.

INFORMATION FRAME TRANSMISSION

After the XPC enters ABM or ABME, the host processor can instruct the XPC to transmit a chain of information frames by issuing the LOAD TRANSMIT TABLE POINTER command. In response, the XPC loads the transmit table pointer and the transmit table function code from the station table into its internal registers. Next, the XPC loads the first transmit buffer pointer, transmit buffer function code, and transmit buffer count from the transmit frame specification table into the corresponding XPC registers. The XPC is now ready to build the first frame.

The remote address is copied from the remote address register into the XPC transmit FIFO. Next the control field is generated and placed in the FIFO. The information field pointed to by the transmit buffer pointer register is then read from the memory buffer into the transmit FIFO until the transmit buffer count is satisfied. A frame check sequence is attached to complete the frame. Zero insertion is performed throughout the transmission. After frame transmission, V(S) is updated and timer T1 is started (if it is not already running) to determine when the programmed time period permitted for a reply to be received has elapsed.

This transmission sequence repeats for each frame until the end of the transmit chain is reached or until the outstanding frames limit is reached. The XPC continues to transmit any available information frames even when the XPC receiver is in the busy condition. The XPC prematurely terminates frame transmission if a link command interrupts the information frame transmission or an error condition arises.

Transmission begins when six bytes are present in the transmit FIFO. Transmission can begin when less than six bytes are present in the FIFO if the entire frame is less than six bytes in length. Between frames, the XPC transmits the user-selected number of pad flags. Additional flags are transmitted if the required number of bytes are not present in the transmit FIFO. While transmitting an information frame, the XPC requests the bus when there are at least six empty bytes in the transmit FIFO unless the last byte of the frame has been loaded into the FIFO.

INFORMATION FRAME RECEPTION

The host processor enables information reception by instructing the XPC to LOAD RECEIVE TABLE POINTER. The XPC will load the receive table pointer and function code into its internal registers. Next, the receive buffer pointer, receive buffer, function code, and the receive buffer count are loaded into the corresponding XPC registers. The XPC is now ready to receive information (I) frames.

The address field of an incoming I-frame is compared to the local address register and the remote address register. If the address does not match the local or remote address, the frame is ignored. If the address field matches the remote address, a frame reject (FRMR) is transmitted and the invalid or unimplemented control field (W) bit of the frame reject descriptor (FRD) register is set. If the address field matches the local address, the frame is accepted by the XPC, and the received N(R) acknowledges previously transmitted I-frames.

Next, the send sequence number, N(S), of the incoming frame is compared to the XPC internal receive state variable, V(R). If the frame is in sequence, then the information field is transferred through the receive FIFO to the receive memory buffer. Out-of-sequence frames are rejected.

Lastly, the XPC performs a CRC check on the incoming information frame. If an error-free frame is received, the XPC acknowledges the frame reception with a supervisory frame (receive ready, RR, or receive not ready, RNR) or with an updated receive sequence number, N(R), in the next information frame.

Zero deletion is performed throughout the reception process. The XPC requests the bus when six bytes are present in the receive FIFO. Only a single frame can reside in the receive FIFO. Frames are received in sequence as long as memory buffers are available.

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XPC STATE DIAGRAM

The XPC state diagram (see Figure 7) is a detailed description of the XPC implementation of the LAPB procedure. The state diagram defines the various XPC states based on command frames received (no errors), response frames received (no errors), and miscellaneous inputs received. For example, if the command received was an RR with the poll bit set to one while in the remote station busy condition (state 9), then the XPC responds with an RR with the final bit set to a one and changes to information transfer (state 5).

STATE	I FRAME WITH POLL	I FRAME W/O POLL	RR WITH POLL	RR W/O POLL	REJ WITH POLL	REJ W/O POLL	RNR WITH POLL	RNR W/O POLL	SABM WITH OR W/O POLL	DISC. WITH OR W/O POLL
S1 DISCONNECTED	DM, F = 1	—	DM, F = 1	—	DM, F = 1	—	DM, F = 1	—	UA, F = P TO S5	DM, F = P
S2 LINK SETUP	—	—	—	—	—	—	—	—	UA, F = P	DM, F = P TO S1
S3 FRAME REJECT	FRMR, F = 1	FRMR, F = 0	FRMR, F = 1	FRMR, F = 0	FRMR, F = 1	FRMR, F = 0	FRMR, F = 1	FRMR, F = 0	UA, F = P TO S5	UA, F = P TO S1
S4 DISCONNECT REQUEST	—	—	—	—	—	—	—	—	DM, F = P TO S1	UA, F = P
S5 INFORMATION TRANSFER	RR, F = 1	**	RR, F = 1	**	RR, F = 1	**	RR, F = 1 TO S9	RR, F = 0 TO S9	UA, F = P	UA, F = P TO S1
S6 REJ FRAME SENT	RR, F = 1 TO S5	** TO S5	RR, F = 1	**	RR, F = 1	**	RR, F = 1 TO S14	RR, F = 0 TO S14	UA, F = P TO S5	UA, F = P TO S1
S7 WAITING I FRAME ACKNOWLEDGE-MENT	RR, F = 1	RR, F = 0	RR, F = 1	RR, F = 0	RR, F = 1	RR, F = 0	RR, F = 1 TO S12	RR, F = 0 TO S12	UA, F = P TO S5	UA, F = P TO S1
S8 STATION BUSY	RNR, F = 1	RNR, F = 0	RNR, F = 1	*N	RNR, F = 1	*N	RNR, F = 1 TO S10	RNR, F = 0 TO S10	UA, F = P	UA, F = P TO S1
S9 REMOTE STATION BUSY	RR, F = 1	RR, F = 0	RR, F = 1 TO S5	** TO S5	RR, F = 1 TO S5	** TO S5	RR, F = 1	RR, F = 0	UA, F = P TO S5	UA, F = P TO S1
S10 BOTH STATIONS BUSY	RNR, F = 1	RNR, F = 0	RNR, F = 1 TO S8	*N TO S8	RNR, F = 1 TO S8	*N TO S8	RNR, F = 1	RNR, F = 0	UA, F = P TO S8	UA, F = P TO S1
S11 WAITING I FRAME ACKNOWLEDGE-MENT AND STA-TION BUSY	RNR, F = 1	RNR, F = 0	RNR, F = 1	RNR, F = 0	RNR, F = 1	RNR, F = 0	RNR, F = 1 TO S13	RNR, F = 0 TO S13	UA, F = P TO S8	UA, F = P TO S1
S12 WAITING I FRAME ACKNOWLEDGE-MENT AND RE-MOTE STATION BUSY	RR, F = 1	RR, F = 0	RR, F = 1 TO S7	RR, F = 0 TO S7	RR, F = 1 TO S7	RR, F = 0 TO S7	RR, F = 1	RR, F = 0	UA, F = P TO S5	UA, F = P TO S1
S13 WAITING I FRAME ACKNOWLEDGE-MENT AND BOTH STATIONS BUSY	RNR, F = 1	RNR, F = 0	RNR, F = 1 TO S11	RNR, F = 0 TO S11	RNR, F = 1 TO S11	RNR, F = 0 TO S11	RNR, F = 1	RNR, F = 0	UA, F = P TO S8	UA, F = P TO S1
S14 REJ FRAME SENT AND REMOTE STATION BUSY	RR, F = 1 TO S9	RR, F = 0 TO S9	RR, F = 1 TO S6	** TO S6	RR, F = 1 TO S6	** TO S6	RR, F = 1	RR, F = 0	UA, F = P TO S5	UA, F = P TO S1

** If I available then Tx I frame else Tx RR, F = 0
*** If I available then Tx I frame else do nothing
*N If I available then Tx I frame else Tx RNR, F = 0
**N If P = 1 then Tx RNR, F = 1 else if I available then Tx I frame else Tx RNR, F = 0
*FR If P = 1 then Tx FRMR, F = 1 else if P = 0 then Tx FRMR, F = 0 else do nothing
*DM If P = 1 then Tx DM, F = 1 else do nothing
*J If no REJ FRAME is outstanding then transmit REJ, F = P else if P = 1 then Tx RR, F = 1 else do nothing
**J If the I field of a correctly received frame has been discarded (due to the busy condition) then Tx REJ, F = 0 else Tx RR, F = 0
— Do nothing
X This event never occurs in this state
UNXF Unexpected final bit

Figure 7. XPC State Diagram

STATE	RR WITH FINAL	RR W/O FINAL	REJ WITH FINAL	REJ W/O FINAL	RNR WITH FINAL	RNR W/O FINAL	UA WITH OR W/O FINAL	DM WITH FINAL	DM W/O FINAL	FRMR WITH OR W/O FINAL	LOCAL START COMMAND
S1 DISCONNECTED	—	—	—	—	—	—	—	SABM TO S2	SABM TO S2	—	SABM TO S2
S2 LINK SETUP	—	—	—	—	—	—	TO S5	TO S1	—	—	X
S3 FRAME REJECT	—	—	—	—	—	—	—	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2
S4 DISCONNECT REQUEST	—	—	—	—	—	—	TO S1	TO S1	—	—	X
S5 INFORMATION TRANSFER	(UNXF) SABM TO S2	***	(UNXF) SABM TO S2	***	(UNXF) SABM TO S2	TO S9	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2
S6 REJ FRAME SENT	(UNXF) SABM TO S2	***	(UNXF) SABM TO S2	***	(UNXF) SABM TO S2	TO S14	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2
S7 WAITING I FRAME ACKNOWLEDGE-MENT	*** TO S5	—	*** TO S5	—	TO S9	TO S12	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2
S8 STATION BUSY	(UNXF) SABM TO S2	***	(UNXF) SABM S2	***	(UNXF) SABM TO S2	TO S10	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2
S9 REMOTE STATION BUSY	(UNXF) SABM TO S2	*** TO S5	(UNXF) SABM TO S2	*** TO S5	(UNXF) SABM TO S2	—	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2
S10 BOTH STATIONS BUSY	(UNXF) SABM TO S2	*** TO S8	(UNXF) SABM TO S2	*** TO S8	(UNXF) SABM TO S2	—	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2
S11 WAITING I FRAME ACKNOWLEDGE-MENT AND STA-TION BUSY	*** TO S8	—	*** TO S8	—	TO S10	TO S13	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2
S12 WAITING I FRAME ACKNOWLEDGE-MENT AND RE-MOTE STATION BUSY	*** TO S5	— TO S7	*** TO S5	— TO S7	— TO S9	—	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2
S13 WAITING I FRAME ACKNOWLEDGE-MENT AND BOTH STATIONS BUSY	*** TO S8	— TO S11	*** TO S8	— TO S11	— TO S10	—	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2
S14 REJ FRAME SENT AND REMOTE STATION BUSY	(UNXF) SABM TO S2	*** TO S6	(UNXF) SABM TO S2	*** TO S6	(UNXF) SABM TO S2	—	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2	SABM TO S2

Figure 7. XPC State Diagram (Continued)

STATE	LOCAL STOP COMMAND	STATION BECOMES BUSY	BUSY CONDITION CLEAR	T1 EXPIRES	N2 × T1 IS EXCEEDED	NS SEQUENCE ERROR	INVALID NR RECEIVED	UNRECOGNIZED FRAME RECEIVED
S1 DISCONNECTED	DISC TO S4	X	—	X	X	*DM	*DM	*DM
S2 LINK SETUP	X	X	—	SABM	TO S1	—	—	—
S3 FRAME REJECT	DISC TO S4	X	—	FRMR F = 0	SABM TO S2	*FR	*FR	*FR
S4 DISCONNECT REQUEST	X	X	—	DISC	TO S1	—	—	—
S5 INFORMATION TRANSFER	DISC TO S4	RNR, F = P TO S8	X	RR, P = 1 TO S7	SABM TO S2	*J TO S6	FRMR(Z) TO S3	FRMR(W) TO S3
S6 REJ FRAME SENT	DISC TO S4	RNR, F = P TO S8	X	RR, P = 1 TO S7	SABM TO S2	IF P = 1 Tx RR, F = 1	FRMR(Z) TO S3	FRMR(W) TO S3
S7 WAITING I FRAME ACKNOWLEDGE-MENT	DISC TO S4	RNR, F = P TO S11	X	RR, P = 1	SABM TO S2	*J	FRMR(Z) TO S3	FRMR(W) TO S3
S8 STATION BUSY	DISC TO S4	X	**J TO S5	RNR, P = 1 TO S11	SABM TO S2	RNR, F = P	FRMR(Z) TO S3	FRMR(W) TO S3
S9 REMOTE STATION BUSY	DISC TO S4	RNR, F = P TO S10	X	RR, P = 1 TO S12	SABM TO S2	*J TO S14	FRMR(Z) TO S3	FRMR(W) TO S3
S10 BOTH STATIONS BUSY	DISC TO S4	X	**J TO S9	RNR, P = 1 TO S13	SABM TO S2	RNR, F = P	FRMR(Z) TO S3	FRMR(W) TO S3
S11 WAITING I FRAME ACKNOWLEDGE-MENT AND STA-TION BUSY	DISC TO S4	X	**J TO S7	RNR, P = 1	SABM TO S2	RNR, F = P	FRMR(Z) TO S3	FRMR(W) TO S3
S12 WAITING I FRAME ACKNOWLEDGE-MENT AND RE-MOTE STATION BUSY	DISC TO S4	RNR, F = P TO S13	X	RR, P = 1	SABM TO S2	*J	FRMR(Z) TO S3	FRMR(W) TO S3
S13 WAITING I FRAME ACKNOWLEDGE-MENT AND BOTH STATIONS BUSY	DISC TO S4	X	**J TO S12	RNR, P = 1	SABM TO S2	RNR, F = P	FRMR(Z) TO S3	FRMR(W) TO S3
S14 REJ FRAME SENT AND REMOTE STATION BUSY	DISC TO S4	RNR, F = P TO S10	X	RR, P = 1 TO S12	SABM TO S2	IF P = 1 Tx RR, F = 1	FRMR(Z) TO S3	FRMR(W) TO S3

Figure 7. XPC State Diagram (Concluded)

XPC TRANSPARENT MODE OF OPERATION

The XPC transparent mode of operation can be used to implement a variety of bit-oriented protocols. The following paragraphs describe the XPC transparent mode of operation.

INITIALIZATION PROCEDURE

The XPC enters the initialization procedure as the result of a hardware or software reset. During initialization, the station table address and function code, system configuration information, and the XPC interrupt vector should be loaded by the XPC under the direction of the host. Note that the XPC will not come out of hardware or software reset without the system clock and the transmit clock. The transmit clock is used to initialize the serial section of the chip.

ENTERING TRANSPARENT OPERATION

Transparent operation is entered when the host issues the MONITOR command. After the monitor command, the XPC asserts $\overline{\text{RTS}}$, transmits flags, and monitors RxD. Since handshaking between nodes is not possible before the monitor command is executed, the host processor at each node must issue the monitor command to enable communication between the two nodes.

FRAME TRANSMISSION

After the MONITOR command is issued, the XPC begins transmission of frames only after receiving a LOAD TRANSMIT TABLE POINTER command from the host. All frames are user generated and may contain user-provided address, control, and/or data fields. After the host issues the LOAD TRANSMIT TABLE POINTER command, the XPC loads the transmit table pointer and the transmit table function code from the station table into its internal registers. Next, the XPC loads the first transmit buffer pointer, transmit buffer function code, and transmit buffer count from the transmit frame specification table into the corresponding XPC registers. The XPC is now ready to transmit the first frame.

The frame pointed to by the transmit buffer pointer register is read from the memory buffer into the transmit FIFO until the transmit buffer count is satisfied. An XPC-generated frame check sequence is then attached to complete the frame. After each frame transmission, the internal V(S) register is incremented without regard to the frame type. This transmission sequence repeats for each frame until the end of the transmit chain is reached. Zero insertion is performed throughout the transmission process.

In transparent operation, the XPC transmits frames until the end of the transmit specification table is reached. After the last frame is transmitted, the XPC sets the IFAK bit in the Tx/link status register to indicate the end of the transmit table. The XPC does not analyze any incoming frames for acknowledgements or link control information during transparent operation. The only errors reported in the Tx/link status register are address error, bus error, clear-to-send lost, and underrun.

Transmission begins when six bytes are present in the transmit FIFO. Transmission can begin when less than six bytes are present in the FIFO if the entire frame is less than six bytes in length. Between frames, the XPC transmits the user-selected number of pad flags. Additional pad flags are transmitted if the required number of bytes are not present in the transmit FIFO for transmission to begin. While transmitting a frame, the XPC requests the bus when there are at least six empty bytes in the transmit FIFO unless the last byte of the frame has been loaded into the FIFO.

FRAME RECEPTION

The host processor enables frame reception by instructing the XPC to LOAD RECEIVE TABLE POINTER. The XPC then loads the receive table pointer and function code into its internal registers. Next, the receive buffer pointer, receive buffer function code, and the receive buffer count are loaded into the corresponding XPC registers. The XPC is now ready to receive frames.

The XPC does not analyze the address and control fields of incoming frames but does perform a CRC check on incoming frames. After the flags are stripped off, the entire frame, including CRC, is written into the current receive buffer, and the RXI bit is set in the Rx/host status register. If a frame is received with a CRC error, the XPC sets the E-bit in that frame's receive specification block. After a frame is received, the XPC increments V(R) without regard to frame type. Zero deletion is performed throughout the reception process.

In transparent operation, the XPC continues to receive frames until the end of the receive specification table is reached. The XPC then sets the RTE bit in the Rx/host status register.

The XPC requests the bus when there are six bytes in the receive FIFO. Only a single frame can reside in the receive FIFO. Frames are received in sequence as long as memory buffers are available.

SIGNAL DESCRIPTION

The input and output signals can be functionally organized into the groups shown in Figure 8.

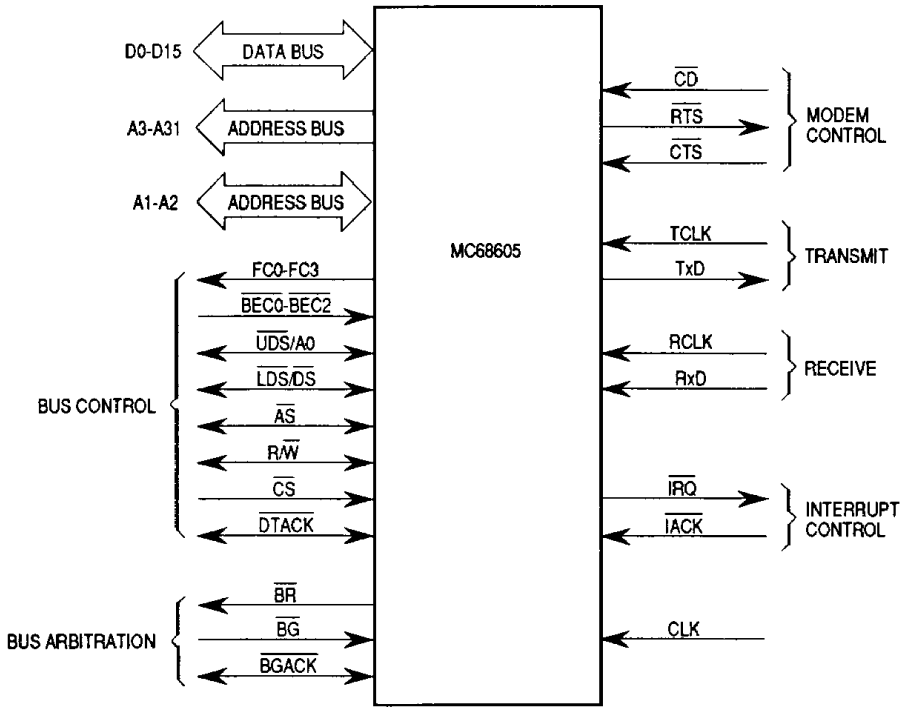

Figure 8. Functional Signal Groups

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ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MC68605 MC68605I	T_A	 0 to 70 0 to 85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance for PGA Thermal Resistance for PLCC	θ_{JA}	33 TBD	°C/W

$T_J = T_A + (P_D \cdot \theta_{JA})$

$P_D = (V_{DD} \cdot I_{DD}) + P_{I/O}$

where:

$P_{I/O}$ is the power dissipation on pins (user determined) which can be neglected in most cases.

For $T_A = 70°C$ and $P_D = 0.55$ W @ 12.5 MHz, $T_J = 88°C$

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = $P_{INT} + P_{PORT}$

P_{INT} = $I_{DD} \times V_{DD}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins, Watts — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

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Solving Equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from Equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS

All specifications are valid under the following conditions: $V_{DD} = 4.75$ V to 5.25 V, $V_{SS} = 0$ V, $T_A = T_L$ to T_H and 130 pF total capacitance on output pins.

Characteristic		Symbol	Min	Max	Unit
Input High Voltage (Except System Clock)		V_{IH}	2.0	V_{DD}	V
Input Low Voltge (Except System Clock)		V_{IL}	$V_{SS}-0.3$	0.8	V
Input High Voltage (System Clock)		V_{CIH}	2.4	V_{DD}	V
Input Low Voltage (System Clock)		V_{CIL}	$V_{SS}-0.3$	0.5	V
Input Leakage Current		I_{in}	—	20	μA
Input Capacitance		C_{in}	—	13	pF
Three-State Leakage Current (2.4/0.5 V)		I_{TSI}	—	20	μA
Open-Drain Leakage Current (2.4 V)		I_{OD}	—	20	μA
Output High Voltage ($I_{OH} = 400$ μA)		V_{OH}	2.4	—	V
Output Low Voltage		V_{OL}			V
($I_{OL} = 3.2$ mA)	A1–A31, FC0–FC3, $\overline{RTS}$, $\overline{TXD}$, $\overline{UDS}$/A0 as A0		—	0.5	
($I_{OL} = 5.3$ mA)	D0–D15, $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$/A0 as $\overline{UDS}$, $\overline{DTACK}$, $\overline{BGACK}$, R/$\overline{W}$		—	0.5	
($I_{OL} = 8.9$ mA)	$\overline{BR}$, $\overline{IRQ}$		—	0.5	
Power Dissipation	@ 10 MHz, 0°C	P_D	—	0.50	W
	@ 12.5 MHz, 0°C		—	0.55	
	@ 16.67 MHz, 0°C		—	0.65	

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AC ELECTRICAL CHARACTERISTICS

High and low outputs are measured at 2.0 V minimum and 0.8 V maximum, respectively. High and low inputs are driven to 2.4 V and 0.5 V, respectively, for AC test purposes. However, input specifications are still measured from 2.0 V to 0.8 V. All specifications are valid under the following conditions: V_{DD} = 4.75 V to 5.25 V, V_{SS} = 0 V, $T_A = T_L$ to T_H, output load = 130 pF, and output current as specified in **DC ELECTRICAL CHARACTERISTICS**; see Figures 9–20.

Num.	Characteristic	10 MHz		12.5 MHz		16.67		Unit
		Min	Max	Min	Max	Min	Max	
1	Asynchronous Input Setup Time	20	—	20	—	10	—	ns
2	$\overline{UDS}$, $\overline{LDS}$ Inactive to $\overline{CS}$, $\overline{IACK}$ Inactive	—	100	—	80	—	60	ns
3	CLK Low (on which $\overline{UDS}$ or $\overline{LDS}$, $\overline{CS}$ or $\overline{IACK}$ Are Recognized) to Data-Out Valid (see Note 5)	— —	1/2 +150	— —	1/2 +120	— —	1/2 +90	Clk. Per. ns
4	$\overline{CS}$ or $\overline{IACK}$ High to Data-Out High Impedance	—	60	—	50	—	35	ns
5	$\overline{LDS}$/$\overline{DS}$ High to Data-Out Hold Time (see Note 6)	0	—	0	—	0	—	ns
6	$\overline{IACK}$ or $\overline{CS}$ Low to $\overline{DTACK}$ High (Driving Three-State $\overline{DTACK}$ High)	—	80	—	70	—	60	ns
7	CLK Low (on which $\overline{UDS}$ or $\overline{LDS}$, $\overline{CS}$ or $\overline{IACK}$ are Recognized) to $\overline{DTACK}$ Low (see Note 5)	— —	2 +90	— —	2 +80	— —	2 +50	Clk. Per. ns
8	CLK Low to $\overline{DTACK}$ Low	—	90	—	80	—	50	ns
9	Data-Out Valid to $\overline{DTACK}$ Low	20	—	20	—	20	—	ns
10	$\overline{DTACK}$ Low to $\overline{UDS}$, $\overline{LDS}$, $\overline{CS}$, $\overline{IACK}$ High (Earliest)	100	—	80	—	60	—	ns
11	$\overline{CS}$ or $\overline{IACK}$ or Data Strobes (the Earliest) High to $\overline{DTACK}$ High (see Note 7)	—	60	—	50	—	40	ns
12	$\overline{DTACK}$ High to $\overline{DTACK}$ High Impedance (At End of Bus Cycle)	—	50	—	50	—	40	ns
13	$\overline{UDS}$, $\overline{LDS}$ Inactive Time	1	—	1	—	1	—	Clk. Per.
14	$\overline{CS}$, $\overline{IACK}$ Inactive Time	0	—	0	—	0	—	ns
15	A1–A2 Valid to $\overline{UDS}$, $\overline{LDS}$, $\overline{CS}$ (the Latest) Low (Write)	30	—	20	—	20	—	ns
16	$\overline{DTACK}$ Low to Data and A1–A2 Hold Time	100	—	80	—	60	—	ns
17	$\overline{UDS}$ or $\overline{LDS}$, $\overline{CS}$ or $\overline{IACK}$ (the Latest) Low to Data-In Valid	—	80	—	70	—	60	ns
18	R/$\overline{W}$ Valid to $\overline{UDS}$ or $\overline{LDS}$, $\overline{CS}$ or $\overline{IACK}$ (Latest) Low	20	—	20	—	10	—	ns
19	$\overline{UDS}$, $\overline{LDS}$ High to R/$\overline{W}$ High	0	—	0	—	0	—	ns
20	CLK High to $\overline{IRQ}$ Low	—	100	—	80	—	60	ns
21	Reserved							
22	Reserved							
23	CLK High to $\overline{BR}$ Low	—	60	—	55	—	40	ns
24	CLK High to $\overline{BR}$ High Impedance	—	55	—	50	—	40	ns
25	$\overline{BGACK}$ Low to $\overline{BR}$ High Impedance	20	—	20	—	10	—	ns
26	$\overline{BG}$ Active/Inactive to CLK Low Setup Time	20	—	20	—	10	—	ns
27	CLK Low to $\overline{BGACK}$ Low	—	60	—	55	—	40	ns
28	CLK High to $\overline{BGACK}$ High Impedance	—	45	—	40	—	40	ns
29	$\overline{AS}$ and $\overline{BGACK}$ High (the Latest) to $\overline{BGACK}$ Low (When $\overline{BG}$ Is Previously Asserted)	2 +20	3 +80	2 +20	3 +70	2 +10	3 +50	Clk. Per. ns
30	$\overline{BG}$ Low to $\overline{BGACK}$ Low (No Other Bus Master)	2 +20	3 +80	2 +20	3 +70	2 +10	3 +50	Clk. Per. ns
31	$\overline{BR}$ High Impedance to $\overline{BG}$ High	0	—	0	—	0	—	ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

Num.	Characteristic	10 MHz		12.5 MHz		16.67 MHz		Unit
		Min	Max	Min	Max	Min	Max	
32	Clock on which $\overline{BGACK}$ Low to Clock on which $\overline{AS}$ Low	1.5	1.5	1.5	1.5	1.5	1.5	Clk. Per.
33	Clock Low to $\overline{BGACK}$ High	—	55	—	50	—	40	ns
34	CLK on which $\overline{BR}$ Low to CLK on which $\overline{BGACK}$ Low (Assuming $\overline{BG}$ Is Active and $\overline{BGACK}$ and $\overline{AS}$ are Inactive for at Least 2 CLK Periods)	1.5	1.5	1.5	1.5	1.5	1.5	Clk. Per.
35	CLK on which $\overline{AS}$ High to CLK on which $\overline{BGACK}$ High	—	1	—	1	—	1	Clk. Per.
36	CLK High to Address Valid	—	100	—	80	—	60	ns
37	CLK High to Address/FC High Impedance	—	70	—	60	—	50	ns
38	CLK High to FC Valid	—	60	—	55	—	50	ns
39	Address Valid to $\overline{AS}$ Valid	20	—	15	—	10	—	ns
40	CLK High to $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$ Low	—	50	—	40	—	40	ns
41	CLK to $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$ High	—	55	—	50	—	40	ns
42	$\overline{AS}$ High to Address/FC Invalid	20	—	10	—	0	—	ns
43	CLK High to $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$ High Impedance	—	70	—	60	—	45	ns
44	CLK to R/$\overline{W}$ High (see Note 4)	—	55	—	50	—	45	ns
45	CLK Low to R/$\overline{W}$ High Impedance	—	70	—	60	—	45	ns
46	$\overline{UDS}$, $\overline{LDS}$ High to Data-In Invalid	0	—	0	—	0	—	ns
47	$\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$ High to $\overline{DTACK}$ High (Earliest of $\overline{AS}$, $\overline{UDS}$, or $\overline{LDS}$)	0	100	0	90	0	60	ns
48	Data-In to CLK Low Setup Time Required when $\overline{DTACK}$ Satisfies (1) (see Note 1)	10	—	10	—	5	—	ns
49	$\overline{DTACK}$ Low to Data-In Valid Required when $\overline{DTACK}$ Does Not Satisfy (1) (see Note 2)	—	65	—	50	—	40	ns
50	CLK High to R/$\overline{W}$ Low	—	60	—	55	—	40	ns
51	$\overline{AS}$ Low to Data-Out Valid (Write)	—	90	—	80	—	60	ns
52	CLK Low to Data-Out Valid	—	55	—	55	—	40	ns
53	Data-Out Valid to $\overline{UDS}$, $\overline{LDS}$ Low	20	—	15	—	10	—	ns
54	$\overline{UDS}$, $\overline{LDS}$ High to Data-Out Invalid	20	—	15	—	0	—	ns
55	CLK High to Data-Out Hold Time	0	100	0	100	0	60	ns
56	No Exception to $\overline{BR}$ ($\overline{DTACK}$ Active)	1.5 +20	2.5 +80	1.5 +20	2.5 +70	1.5 +10	2.5 +50	Clk. Per. ns
57	$\overline{DTACK}$ Low to Asynchronous Exception Active Required when $\overline{DTACK}$ Does Not Satisfy (1) (see Note 2)	—	55	—	35	—	30	ns
58	Exception Active to CLK Low Setup Time Synchronous Input (Late Exception) Required when $\overline{DTACK}$ Satisfies (1) (see Note 1)	45	—	45	—	20	—	ns
59	Exception Active to CLK Low Setup Time Asynchronous Input (Required when $\overline{DTACK}$ Absent) (see Note 3)	20	—	20	—	10	—	ns
60	$\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$ High to Exception Inactive	0	—	0	—	0	—	ns
61	Exception Inactive to CLK Low Setup Time (for Identification of No Exception)	20	—	20	—	10	—	ns
62	No Exception to $\overline{BR}$ ($\overline{DTACK}$ Inactive)	2.5 +20	3.5 +80	2.5 +20	3.5 +70	2.5 +10	3.5 +50	Clk. Per. ns

8

AC ELECTRICAL CHARACTERISTICS (Concluded)

Num.	Characteristic	10 MHz		12.5 MHz		16.67 MHz		Unit
		Min	Max	Min	Max	Min	Max	
63	$\overline{\text{RESET}}$ (on $\overline{\text{BEC0}}$–$\overline{\text{BEC2}}$) Width	10	—	10	—	10	—	Clk. Per.
64	CLK Frequency	4	10	4	12.5	4	16.67	MHz
65	CLK Period	100	250	80	250	60	250	ns
66	CLK Width High (see Note 8)	45	125	35	125	25	125	ns
67	CLK Rise/Fall Time (see Note 8)	—	10	—	5	—	5	ns
68	CLK Width Low (see Note 8)	45	125	35	125	25	125	ns
69	RCLK, TCLK Frequency	0	10	0	12.5	0	16.67	MHz
70	RxD to RCLK High Setup Time	35	—	35	—	25	—	ns
71	RCLK High to RxD Hold Time	5	—	5	—	5	—	ns
72	RCLK, TCLK Rise/Fall Time	—	10	—	10	—	5	ns
73	RCLK, TCLK Width Low	45	—	35	—	25	—	ns
74	RCLK, TCLK Width High	45	—	35	—	25	—	ns
75	RCLK, TCLK Period	100	—	80	—	60	—	ns
76	TCLK Low to TxD Valid	10	80	10	60	10	45	ns
77	Reserved							
78	CD Low to RCLK Low Setup Time	25	—	25	—	25	—	ns
79	CTS Low to TCLK High Setup Time	25	—	25	—	25	—	ns

NOTES:

1. If $\overline{\text{DTACK}}$ satisfies the asynchronous setup time (1), then (48) is required for the data-in setup time and (58) for the synchronous exception setup time. Erroneous behavior may occur if (58) is not satisfied.
2. If $\overline{\text{DTACK}}$ does not satisfy (1), then (49) is required for data-in and (57) for the exception. Erroneous behaviour may occur if (57) is not satisfied.
3. Active exception when $\overline{\text{DTACK}}$ is absent must satisfy the asynchronous setup time (59). Erroneous behavior may occur if (59) is not satisfied.
4. R/$\overline{\text{W}}$ rises on the end of a write cycle (i.e., on the phase following S7). If the XPC relinquishes the bus, then R/$\overline{\text{W}}$ is three-stated one phase later. When the XPC takes the bus, R/$\overline{\text{W}}$ is three-stated until S1 and changes on that phase.
5. Data (3) and $\overline{\text{DTACK}}$ (7) will be timed from the earliest clock on which $\overline{\text{CS}}$ and either data strobe are recognized during an MPU cycle. Data (3) and $\overline{\text{DTACK}}$ will be timed from the earliest clock on which $\overline{\text{IACK}}$ and either data strobe are recognized during an $\overline{\text{IACK}}$ cycle.
6. If $\overline{\text{CS}}$ or $\overline{\text{IACK}}$ is negated before $\overline{\text{UDS}}$/$\overline{\text{LDS}}$, the data bus will be three-stated (4), possibly before $\overline{\text{UDS}}$/$\overline{\text{LDS}}$ negation.
7. If an 8-bit bus is used, only $\overline{\text{LDS}}$ need be considered. If a 16-bit bus is used, both $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$ must negate to apply to this specification.
8. The clock signal during test has 5 ns of rise time and 5 ns of fall time. For system implementations that have less clock rise and fall time, the clock pulse minimum should be commensurately wider such that:
   1. System (TCL + (TCR + TCF) ÷ 2) ≥ (minimum t_{cyc}) ÷ 2
   2. System (TCH + (TCR + TCF) ÷ 2) ≥ (minimum t_{cyc}) ÷ 2

   where
   TCL is CLK width low (see electrical specification #68)
   TCH is CLK width high (see electrical specification #66)
   TCF is CLK rise time
   t_{cyc} is CLK period (see electrical specification #65)
   TCR is CLK fall time

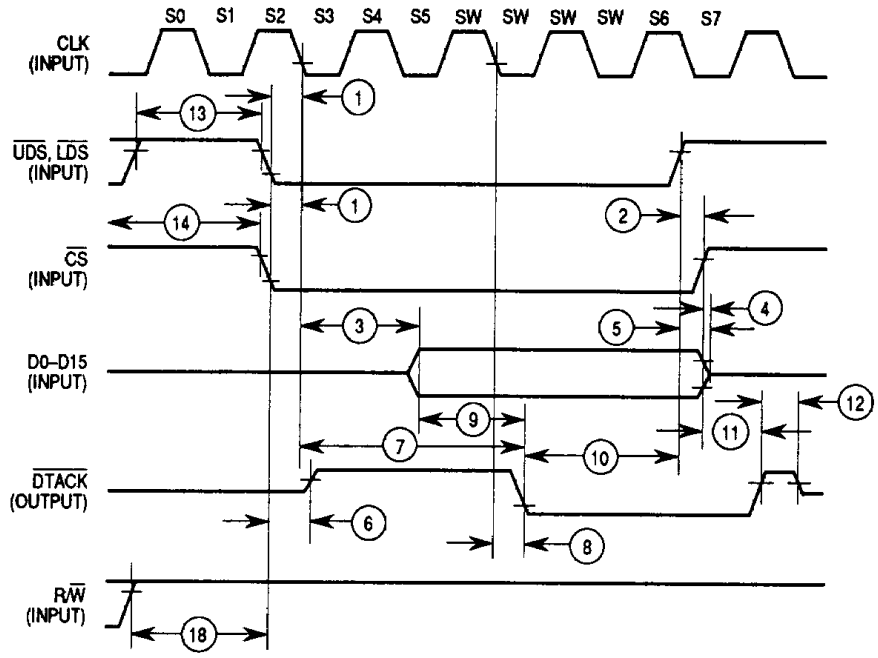


Figure 9. Host Processor Read Cycle Timing Diagram

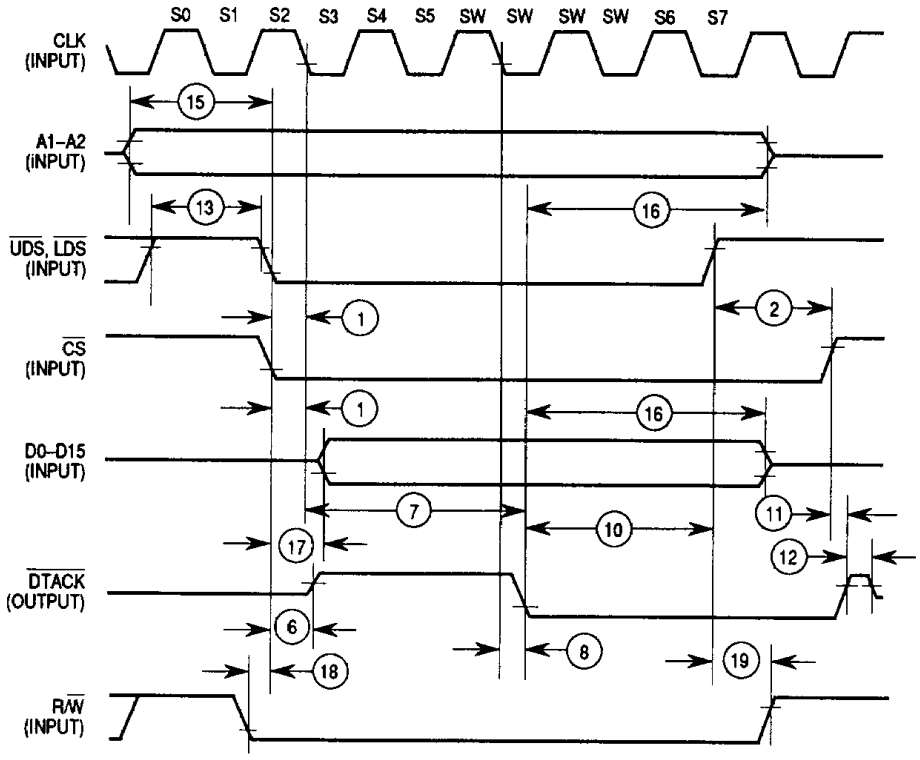


Figure 10. Host Processor Write Cycle Timing Diagram

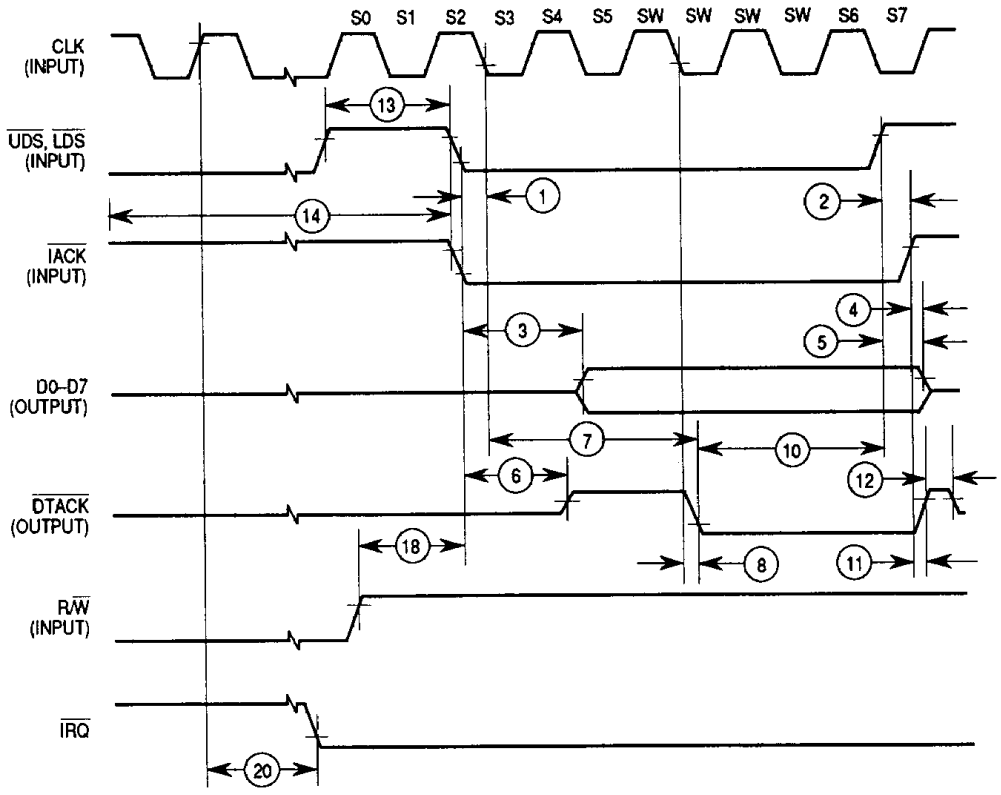


Figure 11. Interrupt Acknowledge Cycle Timing Diagram

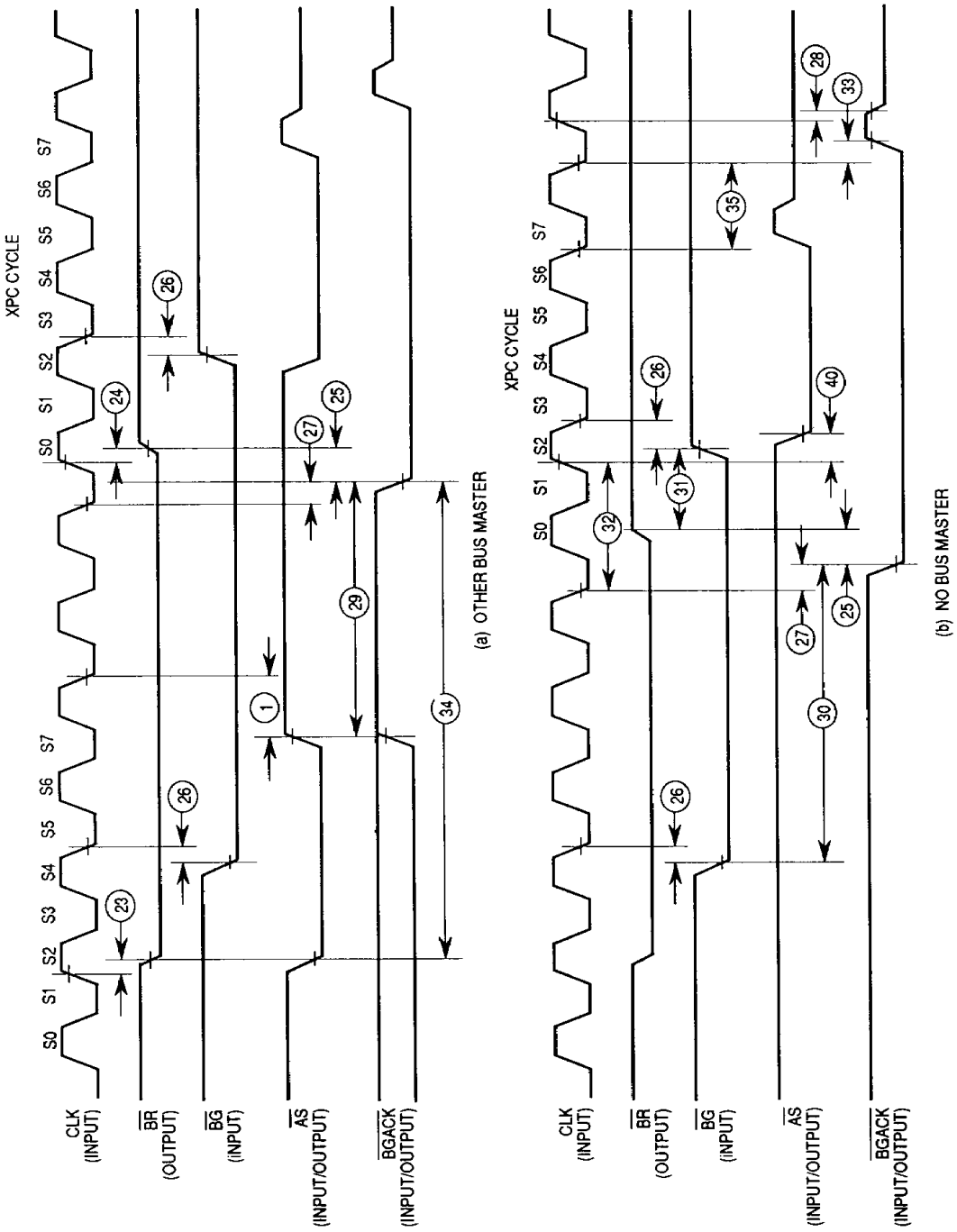
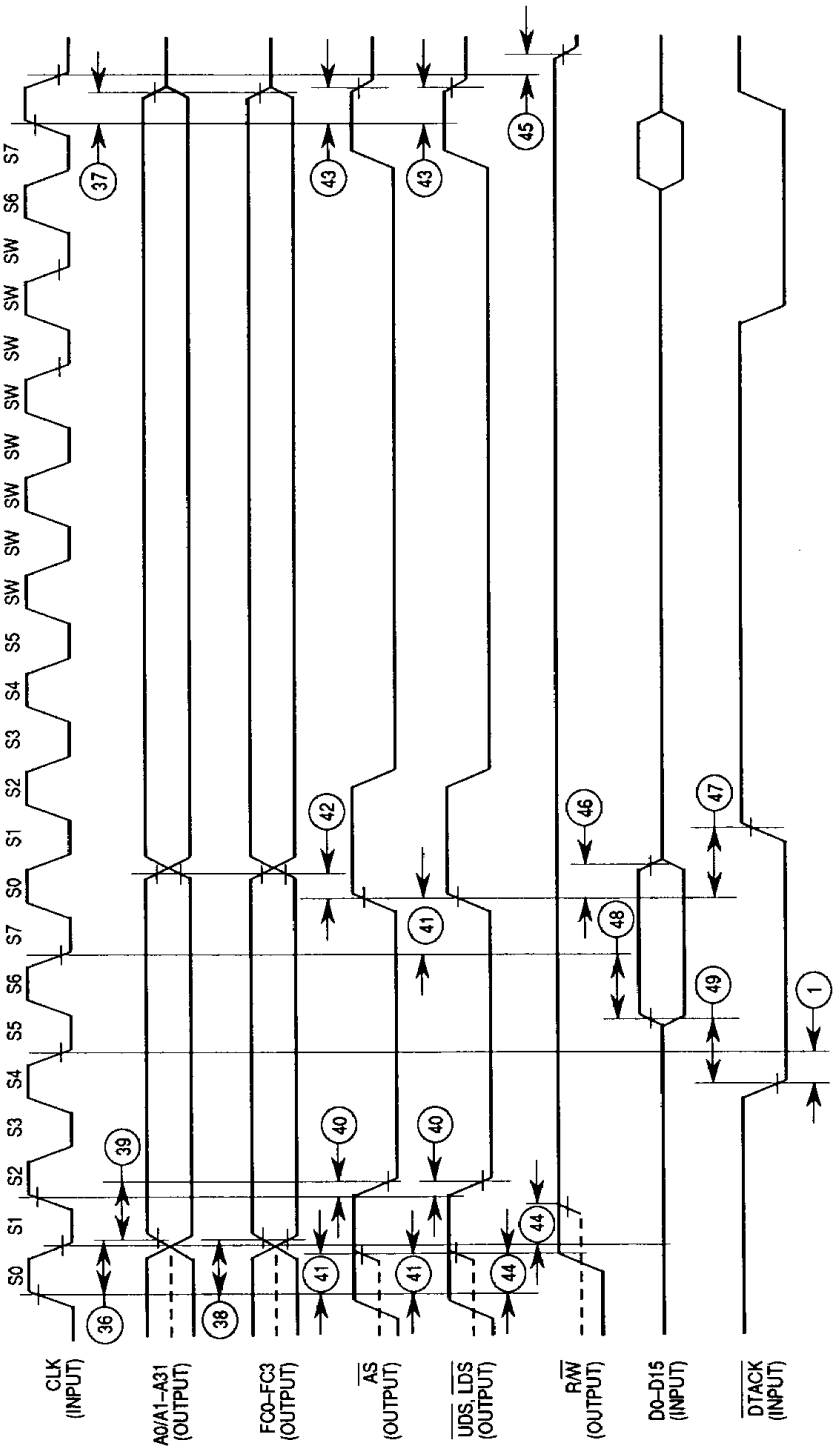


Figure 12. Bus Arbitration Timing Diagram



NOTE: The solid lines assume that the communication controller was bus master on the last cycle. The dotted lines assume that there was a different bus master.

Figure 13. Read Cycle and Slow Read Cycle Timing Diagram

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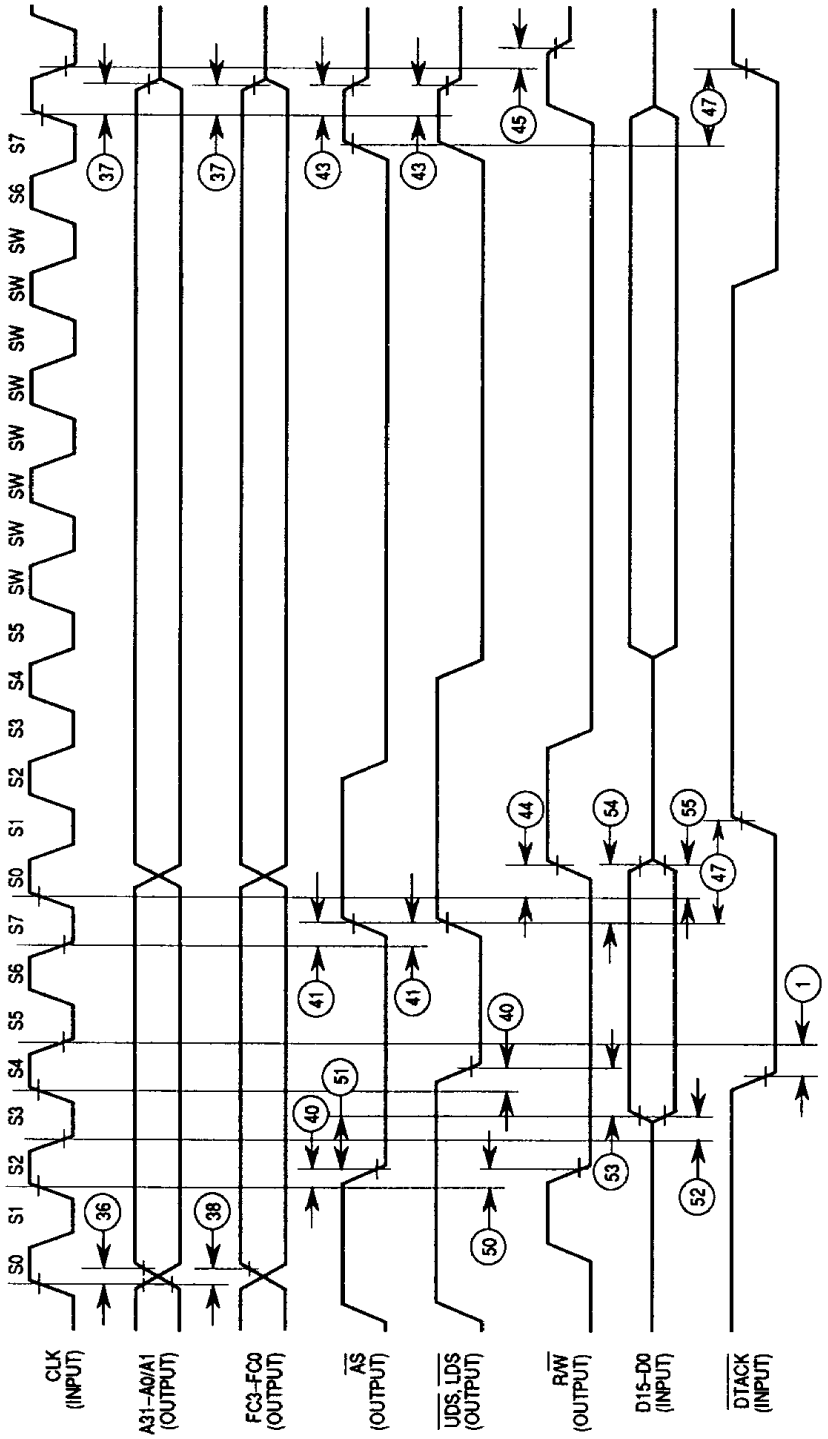
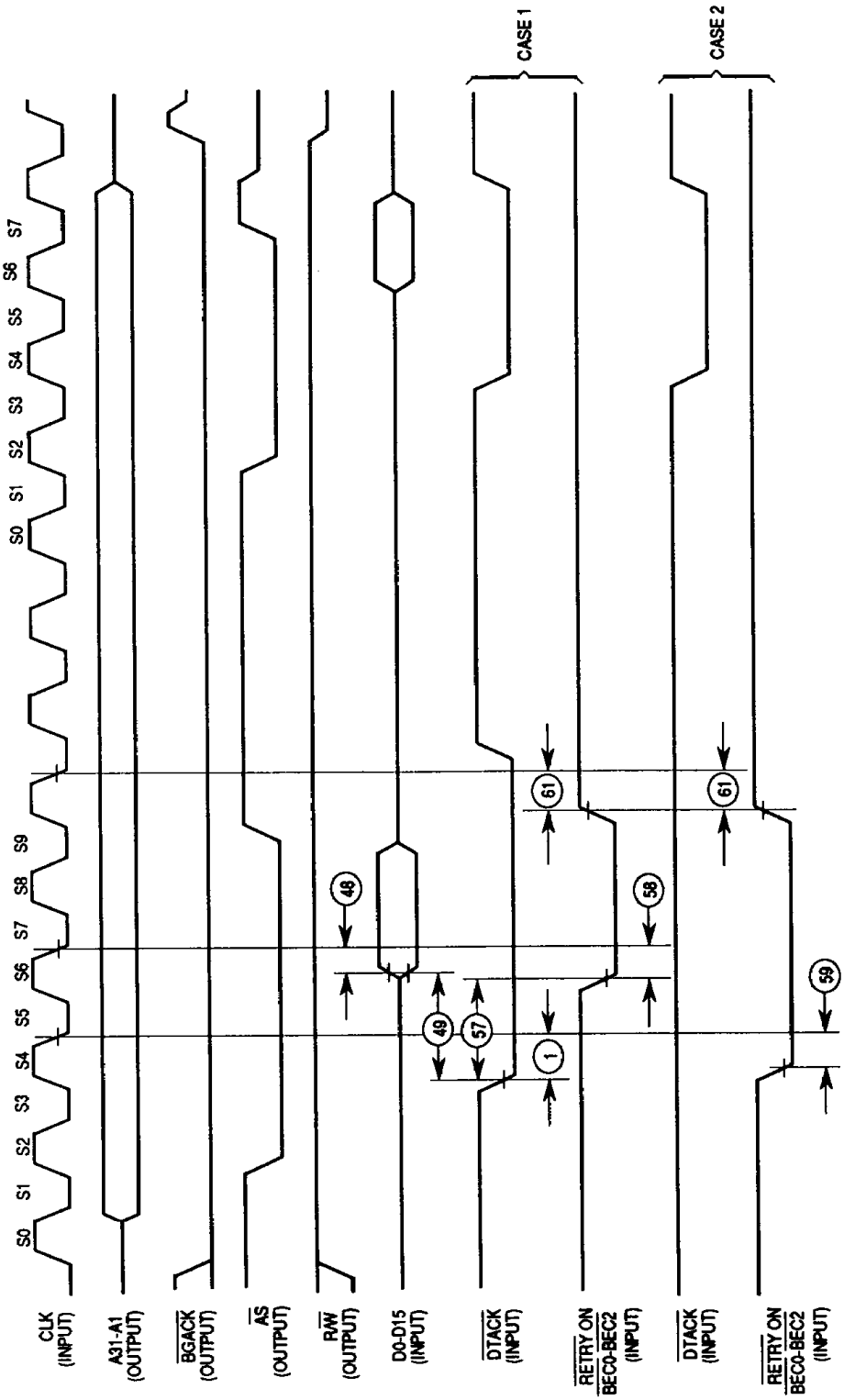


Figure 14. Write Cycle Timing Diagram



Case 1: If DTACK satisfies (1), then (48) and (58) are required; if DTACK is active but does not satisfy (1), then (49) and (57) are required.
Case 2: If DTACK is not active, then (59) is required for the exception active setup time. Parameter (61) is always required for the exception inactive setup time.

Figure 15. XPC Read Cycle with Retry Timing Diagram

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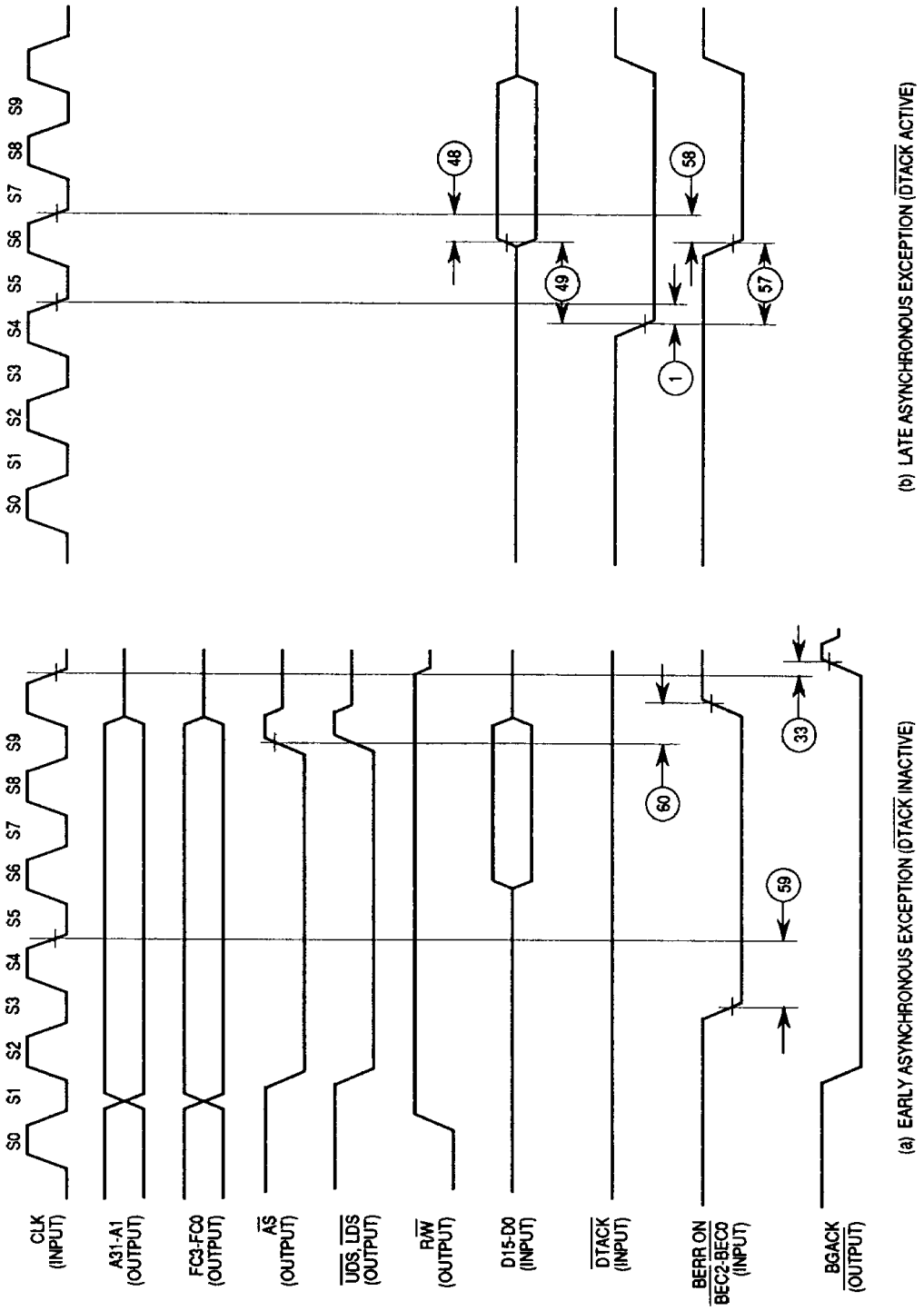
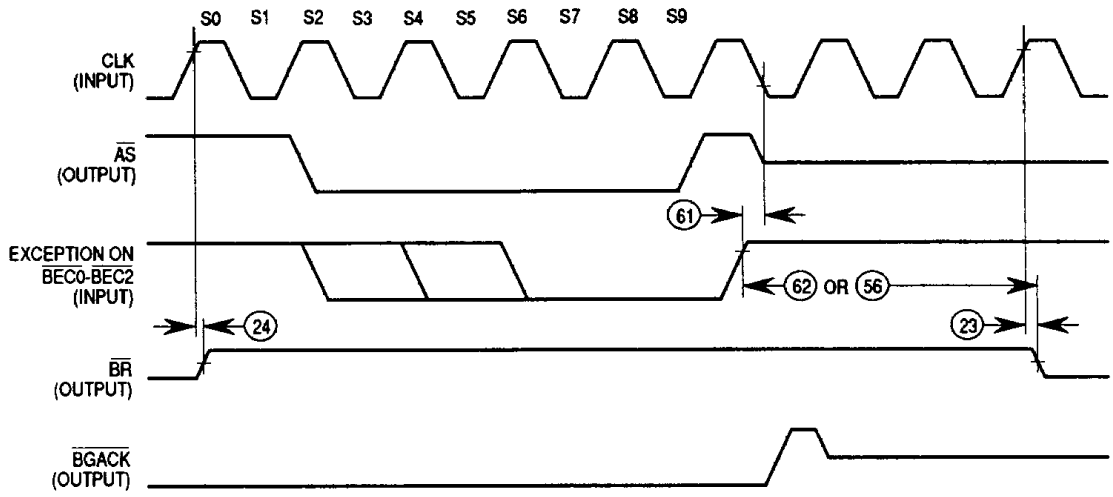
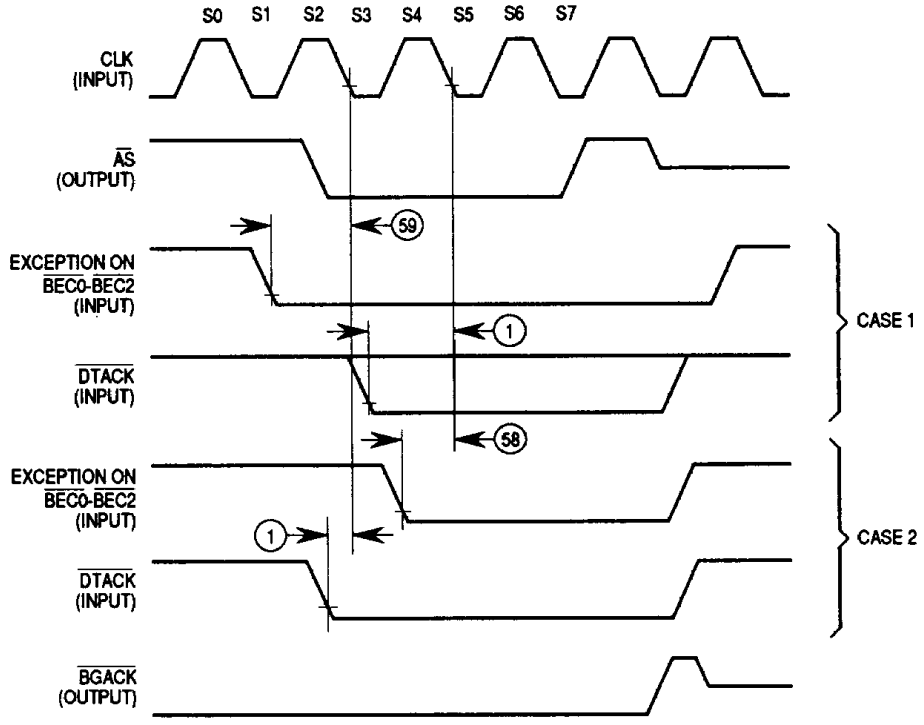


Figure 16. Read Cycle with Bus Error Timing Diagram



NOTE: The above occurs when the XPC requires the bus cycle after a previous exception.

Figure 17. BR after Previous Exception Timing Diagram



NOTE: Two alternatives of DTACK and exception. Case 1 has DTACK occur after exception and case 2 has exception occur after DTACK. Note that a HALT cycle can be terminated only by DTACK.

Figure 18. Short Exception Cycle Timing Diagram

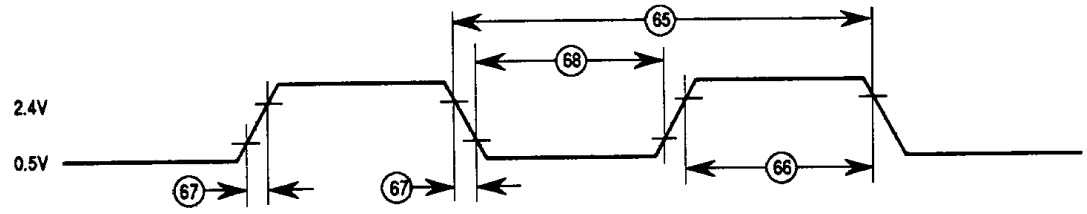


Figure 19. Clock (CLK) Timing Diagram

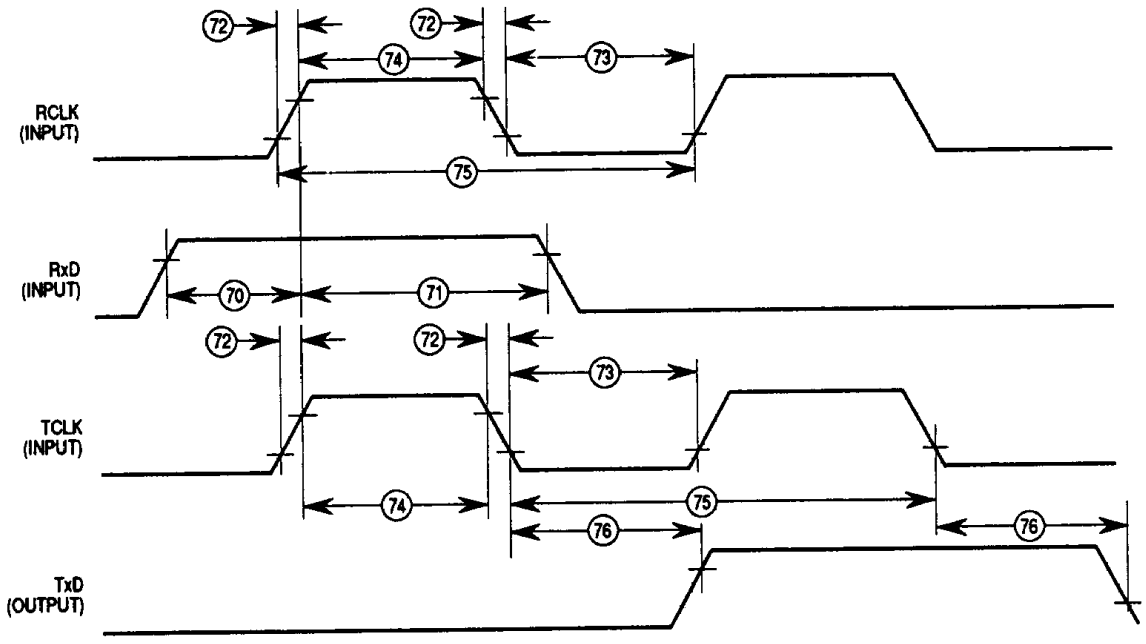
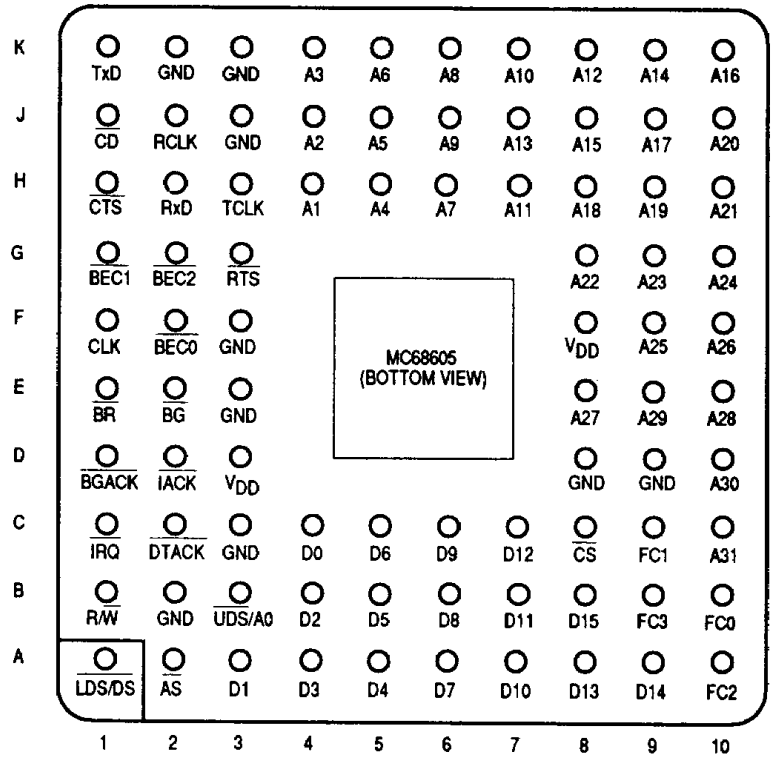


Figure 20. XPC Serial Data RxD, TxD, and Serial Clocks (RCLK, TCLK) Timing Diagram

PIN ASSIGNMENT

84-LEAD PIN GRID ARRAY



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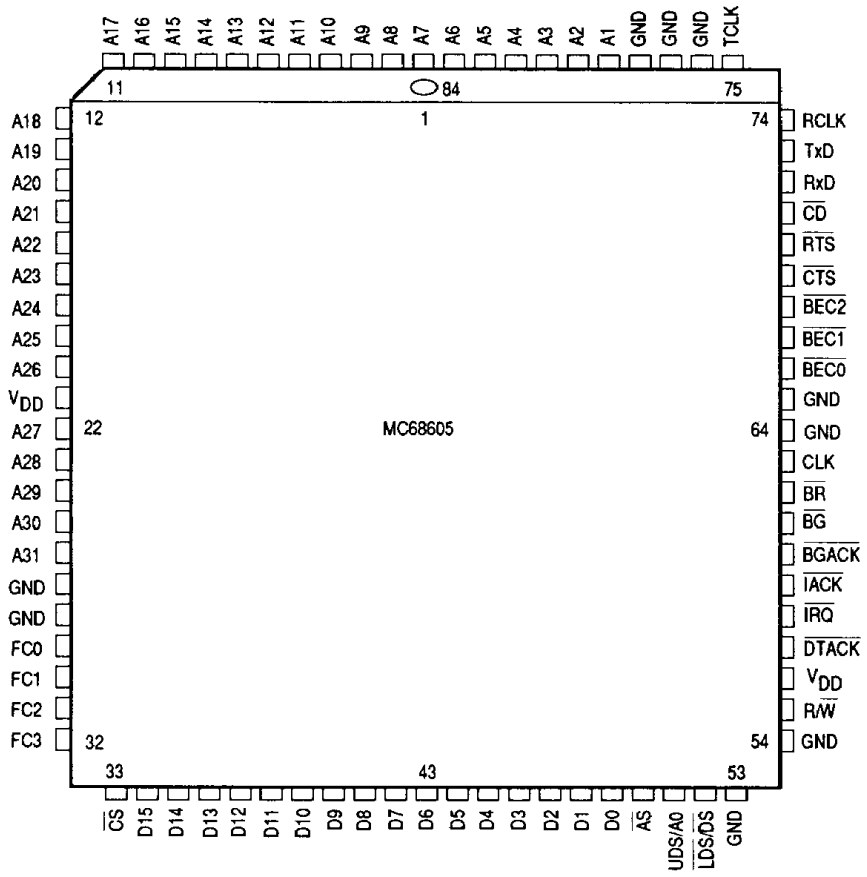
84-LEAD PLASTIC LEADED CHIP CARRIER



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