MB81256-12-W, MB81256-15-W
NMOS 262,144-Bit Dynamic Random Access Memory

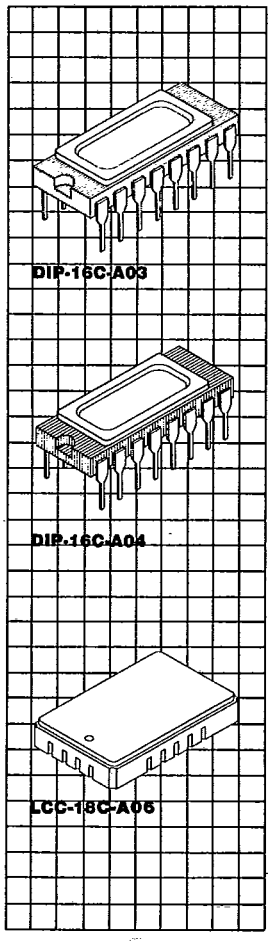
Description

The Fujitsu MB81256-W is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The MB81256-W features "page mode" which allows high speed random access of up to 512-bits within the same row. Additionally, the MB81256-W offers new functional enhancements that make it more versatile than previous dynamic RAMs. Multiplexed row and column address inputs permit the MB81256-W to be housed in a Jedec standard 16-pin dual in-line package and 18-pad LCC.

The MB81256-W is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including dynamic sense amplifiers.

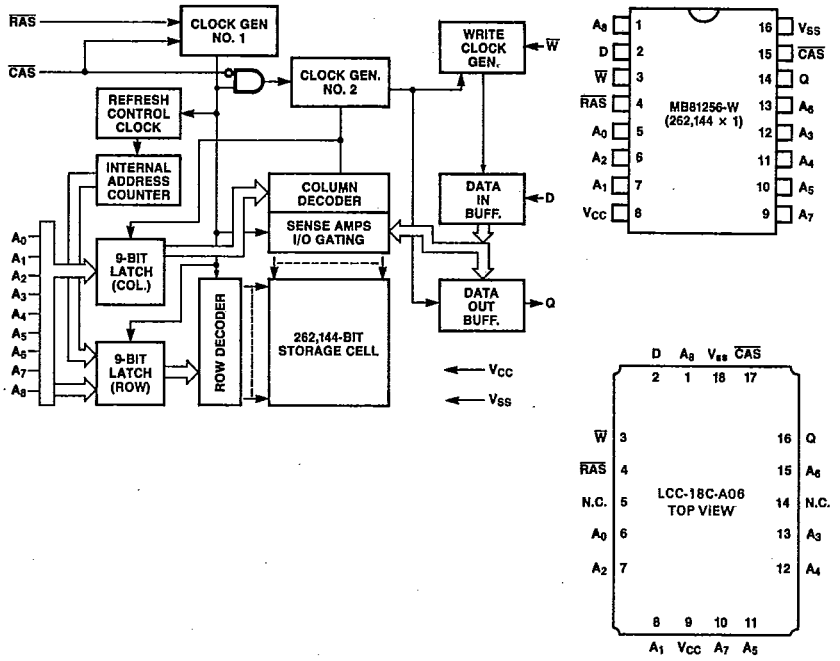
Clock timing requirements are noncritical, and the power supply tolerance is very wide. All inputs are TTL compatible.



Features

- Wide temperature range: T_C = −55°C to +110°C
- 262,144 x 1-bit organization
- Row Access Time/Cycle Time:
  MB81256-12-W
  120 ns max./250 ns min.
  MB81256-15-W
  150 ns max./280 ns min.
- Page cycle time
  MB81256-12-W 120 ns max.
  MB81256-15-W 150 ns max.
- Low Power Dissipation:
  347 mW max. (t_{RC} = 280 ns)
  33 mW (Standby)
- +5V supply voltage, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- Common I/O capability using "Early Write" operation
- On-chip substrate bias generator
- Page Mode Capability
- Fast Read-Write Cycle, $t_{RWC} = t_{RC}$
- t_{AR}, t_{WCR}, t_{DHR}, t_{RWD} eliminated
- $\overline{CAS}$-before-$\overline{RAS}$ on chip refresh
- Hidden $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh
- $\overline{RAS}$-only refresh
- 2 ms/256 cycle refresh
- Output unlatched at cycle end allows two dimensional chip select
- On-chip Address and Data-in latches
- Industry standard 16-pin package

MB81256 Block Diagram and Pin Assignments



Note: The following IEEE Std. 662-1980 symbols are used in this data sheet: D = Data In, $\overline{W}$ = Write Enable, Q = Data Out.

Absolute Maximum Ratings

(See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−1.0 to 7.0	V
Operating temperature (case)	T_{OP}	−55 to 110	°C
Storage temperature	T_{STG}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage high than maximum rated voltages to this high impedance circuit.

Description

Simplifed Timing Requirement

The MB81256-W has improved circuitry that eases timing requirements for high speed access operations. The MB81256-W can operate under the condition of t_{RCD} (max) = t_{CAC}, thus providing optimal timing for address multiplexing. In addition, the MB81256-W has minimal hold times for Addresses (t_{CAH}), Write-Enable (t_{WCH}) and Data-in (t_{DH}). The MB81256-W provides higher throughput in inter-leaved memory system applications. Fujitsu has made the timing requirements that are referenced to $\overline{RAS}$ nonrestrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Fast Read-Write Cycle

The MB81256-W has a fast read-modify-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes "low". When $\overline{W}$ is "low" during a $\overline{CAS}$ transition to "low", the MB81256-W goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. When $\overline{W}$ goes "low", the MB81256-W goes into the delayed write mode. The output then contains the data from the cell selected and the data from D is written into the cell selected. Therefore, a very fast read-write cycle (t_{RWC} = t_{RC}) is possible with the MB81256-W.

Address Inputs

A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB81256-W. Nine row-address bits are established on the input pins (A_0 through A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold/time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable

The read or write mode is selected with the $\overline{W}$ input. A logic "high" on $\overline{W}$ dictates write mode. The data input is disabled when the read mode is selected.

Data Input

Data is written into the MB81256-W during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the data-in (D) register. In a write cycle, if $\overline{W}$ is brought "low" (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Page Mode

Page mode operation permits strobing the row address into the MB81256-W while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row address doesn't change. Thus, the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

$\overline{RAS}$-Only Refresh

Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 ~ A_7) at least every 2 ms. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought "low". Strobing each of the 256 row-addresses (A_0 ~ A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh

$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB81256-W offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh

A hidden refresh cycle may take place while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time. For the MB81256-W, a hidden refresh cycle is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counter provides the refresh addresses as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

Description
(Continued)

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to "high" and then goes to "low" again while $\overline{RAS}$ is held "low", the read and write operation are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

A Row Address

Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.

A Column Address

All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all the following operations:

1) Initialize the internal refresh counter. For this operation, 8 cycles are required.
2) Write a test pattern of "low"s into memory cells at a single column address and 256 row address.
3) Using a read-modify-write cycle, read the "low" written at the last operation (Step 2) and write a new "high" in the same cycle. This cycle is repeated 256 times, and "high"s are written into the 256 memory cells.
4) Read the "high"s written at the last operation (Step 3).
5) Complement the test pattern and repeat steps (2), (3) and (4).

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Value Min	Typ	Max	Unit	Operating Temperature (T_C)
Supply voltage	V_{CC}	4.5	5.0	5.5	V	−55°C to +110°C (case)
	V_{SS}	0	0	0	V	
Input high voltage all inputs	V_{IH}	2.4		6.5	V	
Input low voltage all inputs	V_{IL}	−2.0		0.8	V	

Capacitance
(T_A = 25°C)

Parameter	Symbol	Value Min	Typ	Max	Unit
Input capacitance A_0 to A_8, D	C_{IN1}			7	pF
Input capacitance $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$	C_{IN2}			10	pF
Output capacitance Q	C_{OUT}			7	pF

DC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81256-12-W Min	MB81256-12-W Max	MB81256-15-W Min	MB81256-15-W Max	Unit
Operating current*1 Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		72		63	mA
Standby current Power supply current ($\overline{RAS}$/$\overline{CAS}$ = V_{IH})	I_{CC2}		6.0		6.0	mA
Refresh current*1 Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		61		55	mA
Page mode current*1 Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		33		28	mA
Refresh current 2*1 Average power supply current ($\overline{CAS}$ before $\overline{RAS}$, t_{RC} = min.)	I_{CC5}		66		61	mA
Input leakage current Any input, (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	μA
Output leakage current (Data is disabled, V_{OUT} = 0V to 5.5V)	I_{OL}	−10	10	−10	10	μA
Output level Output low voltage (I_{OL} = 4.2 mA)	V_{OL}		0.4		0.4	V
Output level Output high voltage (I_{OH} = −5.0 mA)	V_{OH}	2.4		2.4		V

Note: *1 I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol Alternate	Symbol *Standard	MB81256-12-W Min	MB81256-12-W Max	MB81256-15-W Min	MB81256-15-W Max	Unit
Time between refresh	t_{REF}	TRVRV		2		2	ms
Random read/write cycle time	t_{RC}	TRELREL	250		280		ns
Read-write cycle time	t_{RWC}	TRELREL	250		280		ns
Access time from $\overline{RAS}$*4,6	t_{RAC}	TRELQV		120		150	ns
Access time from $\overline{CAS}$*5,6	t_{CAC}	TCELQV		60		75	ns
Output buffer turn off delay	t_{OFF}	TCEHQZ	0	25	0	30	ns
Transition time	t_T	TT	3	50	3	50	ns

Notes: *1 An initial pause of 200μs is required after power up, followed by any 8 $\overline{RAS}$ cycles, before proper device operation is achieved. If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh initialization cycles are required.

*2 AC characteristics assume t_T = 5ns.

*3 V_{IH} (min.) and V_{IL} (max.) are reference levels measured between V_{IH} and V_{IL}.

*4 t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (max.) the specified maximum value of t_{RAC} (max.) can be met. If $t_{RCD} > t_{RCD}$ (max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (max.)

*5 Assumes that $t_{RCD} > t_{RCD}$ (max.).

*6 Measured with a load equivalent to 2 TTL loads and 100 pF.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol Alternate	Symbol *Standard	MB81256-12-W Min	MB81256-12-W Max	MB81256-15-W Min	MB81256-15-W Max	Unit
$\overline{RAS}$ precharge time	t_{RP}	TREHREL	120		120		ns
$\overline{RAS}$ pulse width	t_{RAS}	TRELREH	120	10000	150	10000	ns
$\overline{RAS}$ hold time	t_{RSH}	TCELREH	60		75		ns
$\overline{CAS}$ pulse width	t_{CAS}	TCELCEH	60	10000	75	10000	ns
$\overline{CAS}$ hold time	t_{CSH}	TRELCEH	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time*4,7	t_{RCD}	TRELCEL	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	TCEXREL	20		20		ns
Row address set up time	t_{ASR}	TAVREL	0		0		ns
Row address hold time	t_{RAH}	TRELAX	12		15		ns
Column address set up time	t_{ASC}	TAVCEL	0		0		ns
Column address hold time	t_{CAH}	TCELAX	20		25		ns
Read command set up time	t_{RCS}	TWHCEL	0		0		ns
Read command hold time referenced to $\overline{CAS}$*9	t_{RCH}	TCEHWX	0		0		ns
Read command hold time referenced to $\overline{RAS}$*9	t_{RRH}	TREHWX	20		20		ns
Write command set up time*8	t_{WCS}	TWLCEL	0		0		ns
Write command pulse width	t_{WP}	TWLWH	20		25		ns
Write command hold time	t_{WCH}	TCELWH	20		25		ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	TWLREH	50		60		ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	TWLCEH	50		60		ns
Data in set up time	t_{DS}	TDVCEL	0		0		ns
Data in hold time	t_{DH}	TCELDX	20		25		ns
$\overline{CAS}$ to $\overline{W}$ delay*8	t_{CWD}	TCELWL	20		25		ns
Refresh set up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	TCELREL	25		30		ns
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	TRELCEX	25		30		ns
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	TREHCEL	20		20		ns
Page mode read/write cycle time	t_{PC}	TCELCEL	120		150		ns
Page mode read-write cycle time	t_{PRWC}	TCEHCEH	120		150		ns
Page mode $\overline{CAS}$ precharge time	t_{CP}	TCEHCEL	50		65		ns
$\overline{CAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CPR}	TCEHCEL	25		30		ns

Notes: *These symbols are described in IEEE STD. 662-1980: IEEE Standard terminology for semiconductor memory.

*4 t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (max.) the specified maximum value of t_{RAC} (max.) can be met. If $t_{RCD} > t_{RCD}$ (max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (max.)

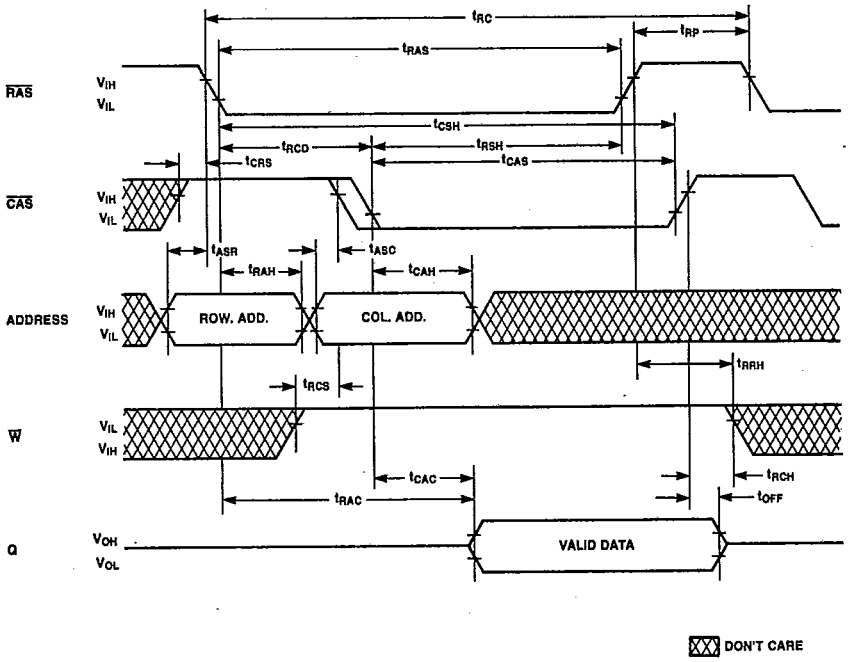
*7 t_{RCD} (min.) = t_{RAH} (min.) + $2t_T$ + t_{ASC} (min.).

*8 t_{WCS} and t_{CWD} are non restrictive operating parameters, and are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle, and the data out pin will remain open circuit (High Impedance) throughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.

*9 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

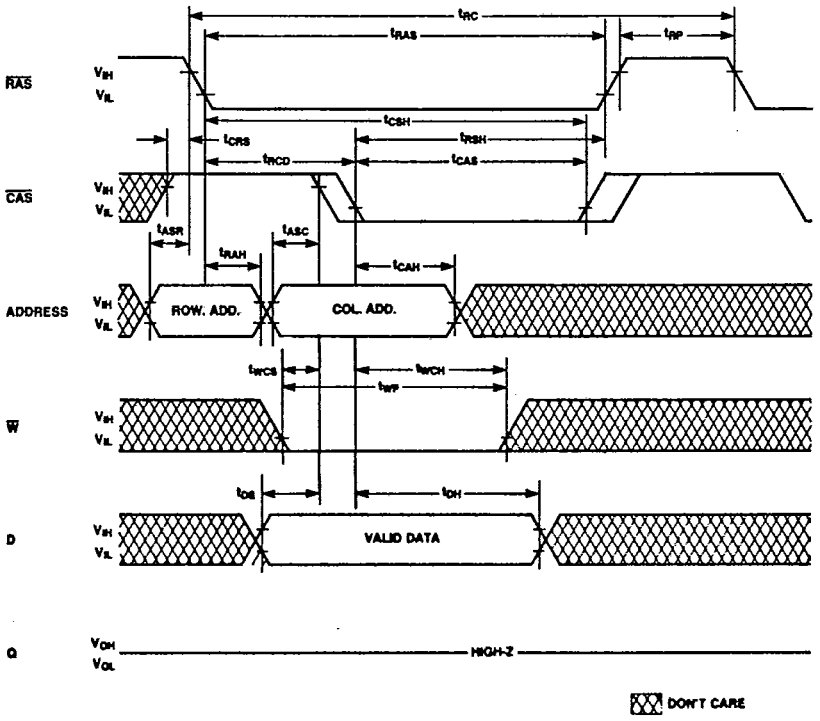
Timing Diagrams

Read Cycle



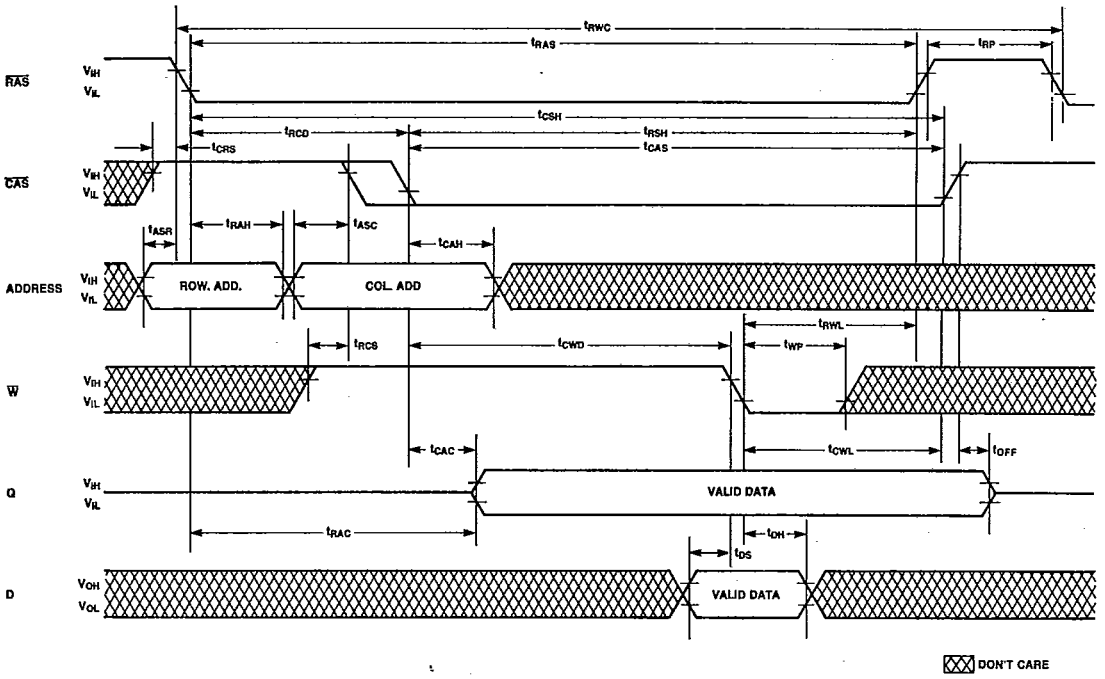
Timing Diagrams
(Continued)

Write Cycle (Early Write)



Timing Diagrams
(Continued)

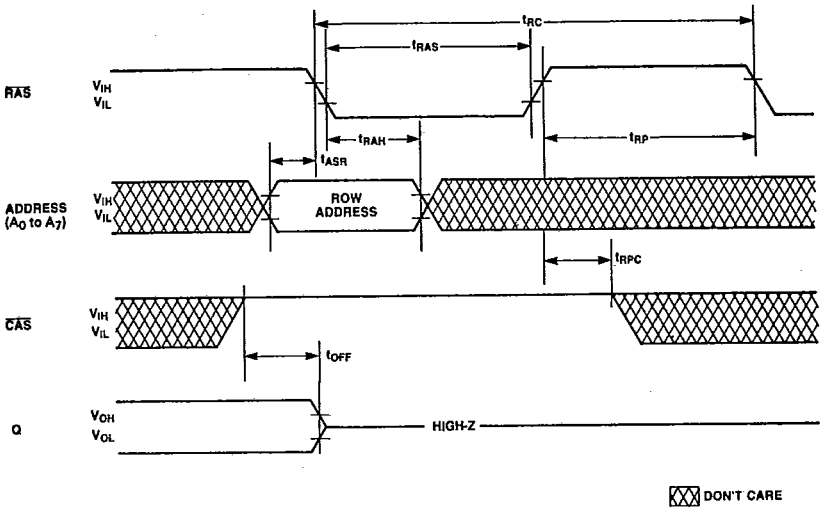
Read-Write/Read-Modify-Write Cycle



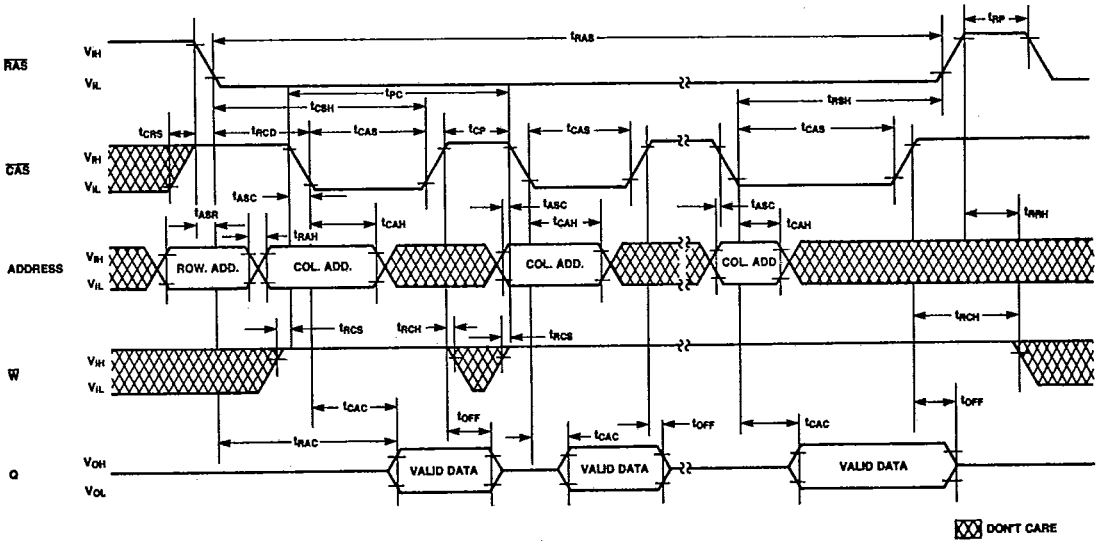
Timing Diagrams
(Continued)

"RAS-Only" Refresh Cycle

Note: $\overline{CAS}$ = V_{IH}, $\overline{W}$, D = Don't Care, A_8 = V_{IL} or V_{IH}

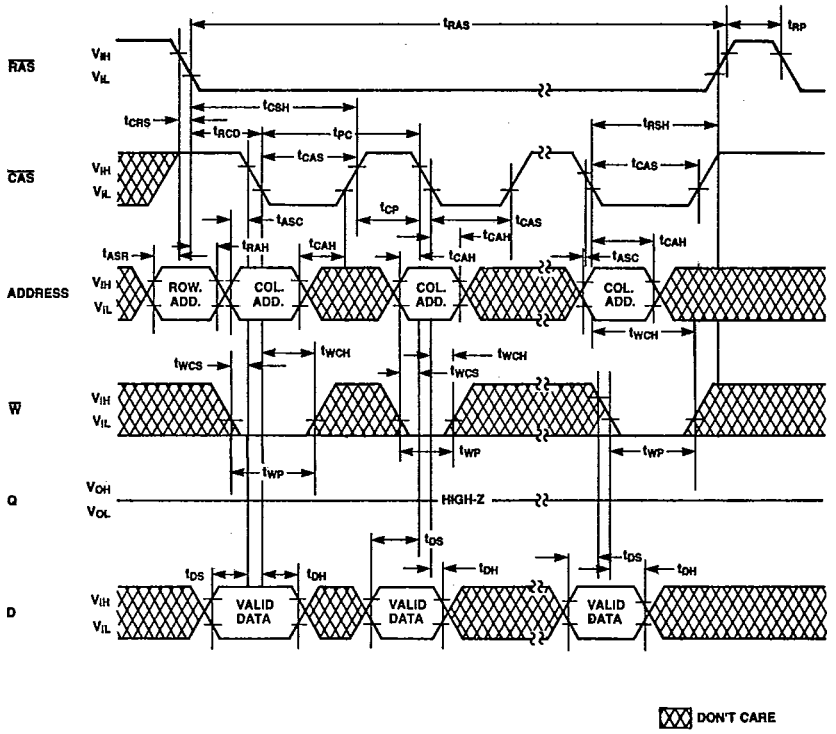


Page Mode Read Cycle



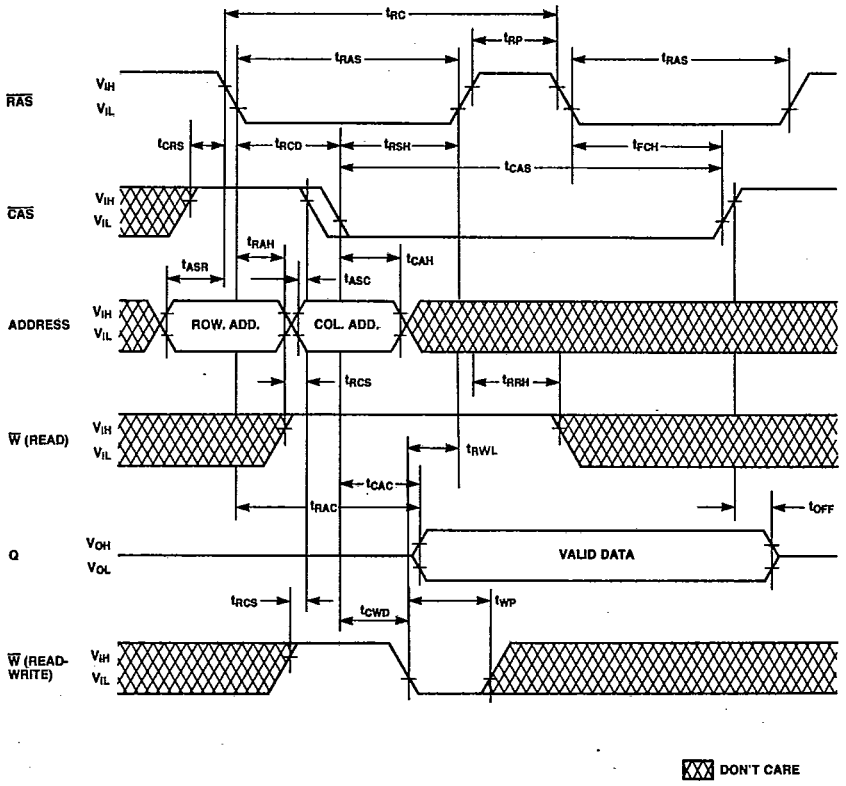
Timing Diagrams
(Continued)

Page Mode Write Cycle



Timing Diagrams
(Continued)

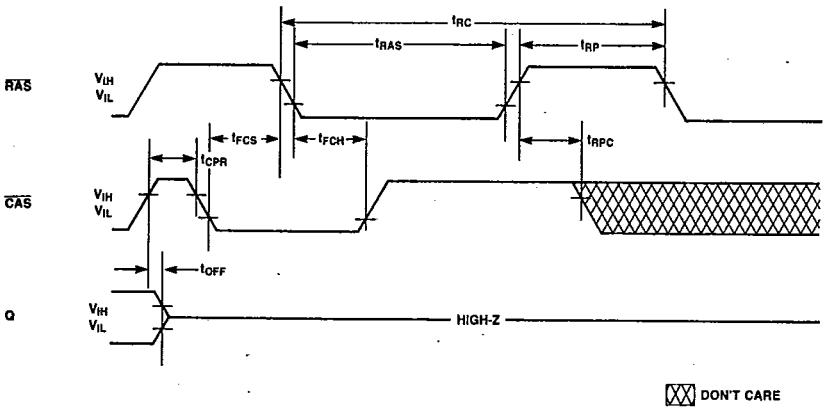
Hidden Refresh Cycle



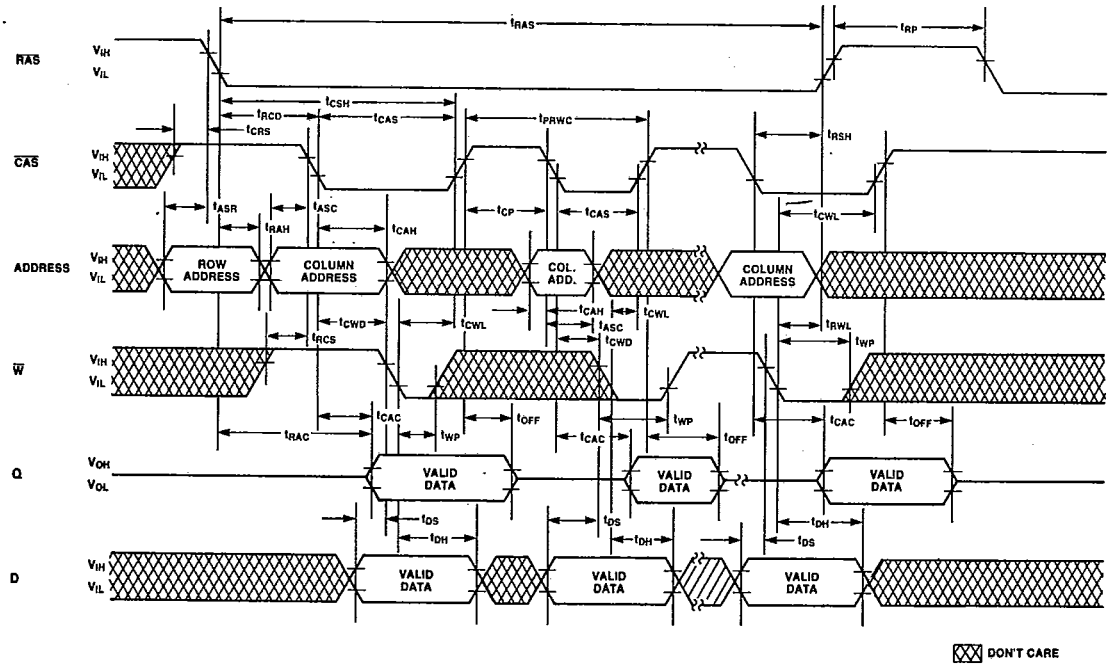
Timing Diagrams
(Continued)

"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Cycle

Note: A, $\overline{W}$, D = Don't Care

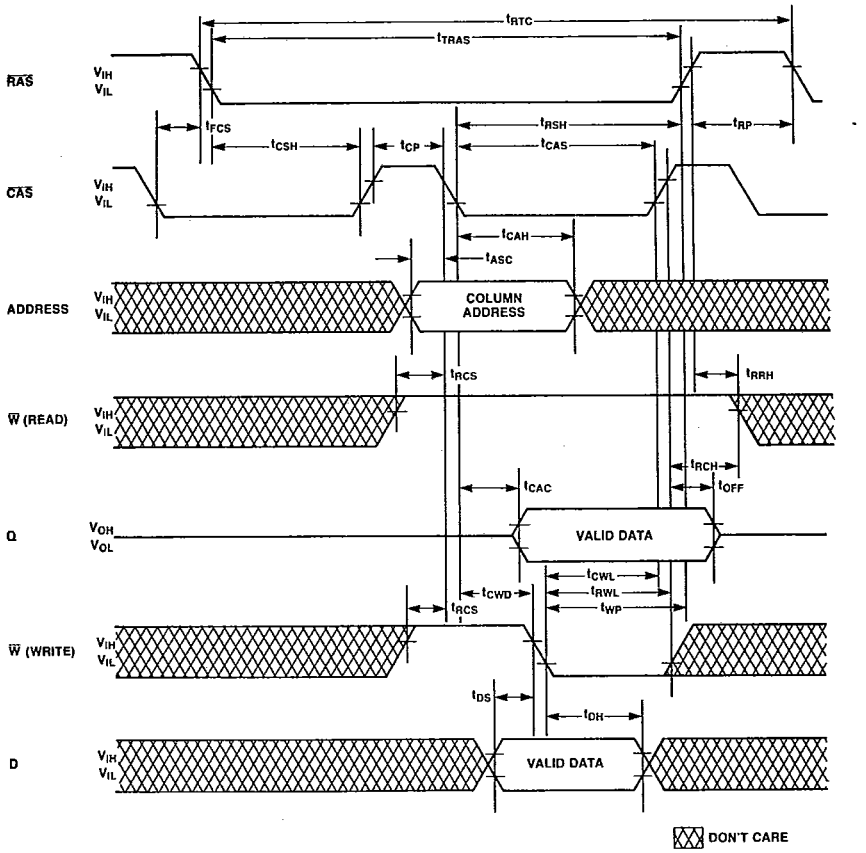


Page Mode Read-Write Cycle



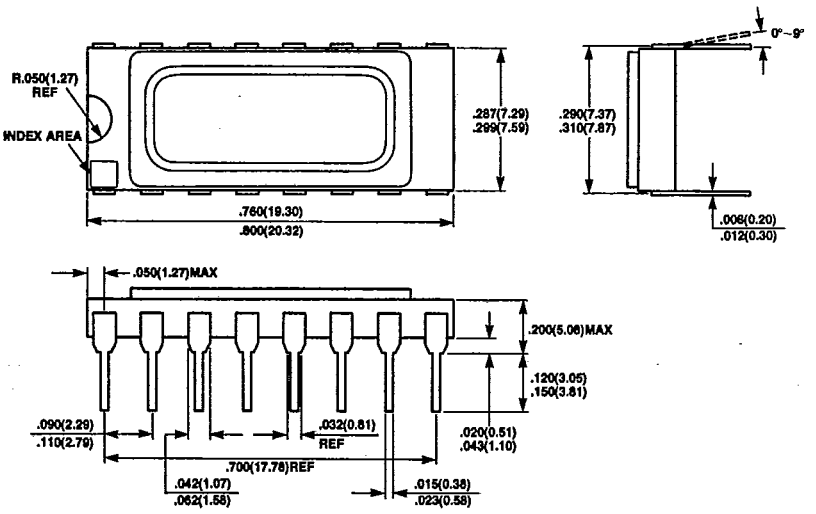
Timing Diagrams
(Continued)

"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Counter Test Cycle

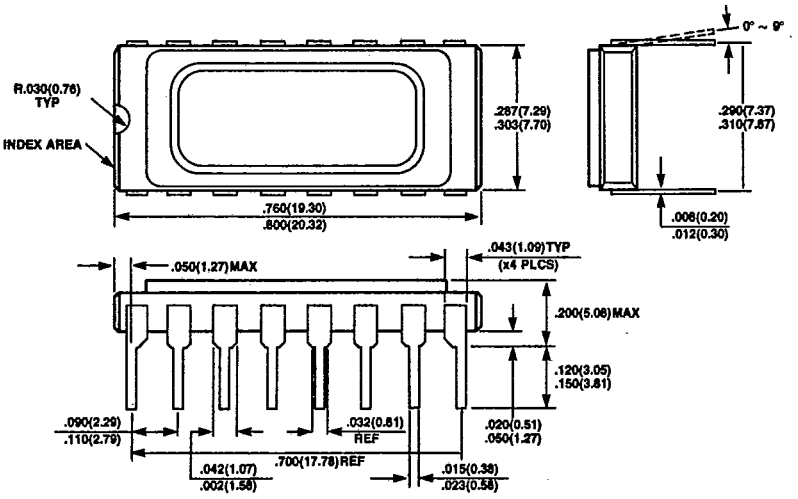


Package Dimensions
Dimensions in inches
(millimeters)

16-Lead Ceramic (Metal Seal) Dual In-Line Package
(Case No.: DIP-16C-A03)



16-Lead Seam Weld Dip Package
(Case No.: DIP-16C-A04)



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

18-Pad Ceramic Leadless Chip Carrier
LCC-18C-A06)