

Ordering number: EN2361

CMOS LSI

**SANYO** **LC3517A, AM, AS, AL, AML, ASL**  
**2048-word × 8-bit CMOS Static RAM**

**OVERVIEW**

LC3517A series devices are silicon-gate CMOS, static RAM ICs configured as 2048 words × 8 bits. They incorporate an output enable for high-speed memory access, and TTL-compatible, tristate outputs for direct interfacing with a bus.

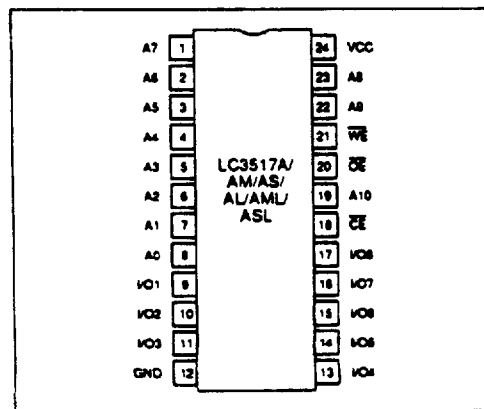
LC3517A series ICs feature a data retention mode and a low standby current, making them ideal for low-power or battery-powered equipment. In particular, the LC3517AL, LC3517AML and LC3517ASL offer a guaranteed maximum standby current of 1 µA at 60 deg. C.

LC3517A series ICs operate from a 5 V supply and are available in 24-pin DIPs, 24-pin MFPs and 24-pin SDIPs.

**FEATURES**

- 100 ns (LC3517A-10 series), 120 ns (LC3517A-12 series) and 150 ns (LC3517A-15 series) maximum address access times
- 0.2 µA at 25 deg. C and 1.0 µA at 60 deg. C (LC3517AL/AML/ASL-10/12/15), and 5.0 µA at 60 deg. C and 30 µA at 85 deg. C (LC3517A/AM/ASL-10/12/15) maximum standby currents
- 55 mA maximum supply current at f = 1 MHz
- Data retention for V<sub>CC</sub> = 2.0 to 5.5 V
- Asynchronous operation
- TTL-compatible, tristate input/outputs
- Single 5 V supply
- 24-pin DIP, 24-pin MFP and 24-pin SDIP

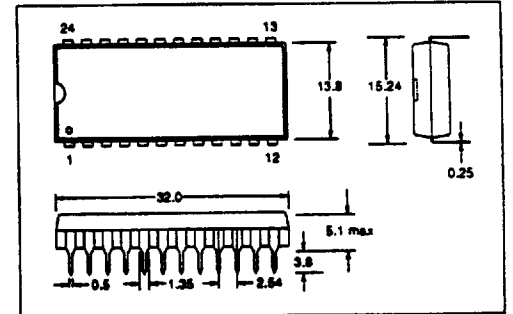
**PINOUT**



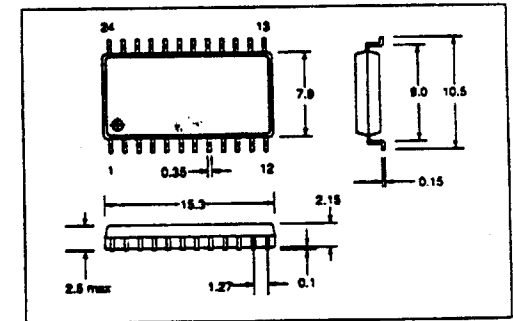
**PACKAGE DIMENSIONS**

Unit: mm

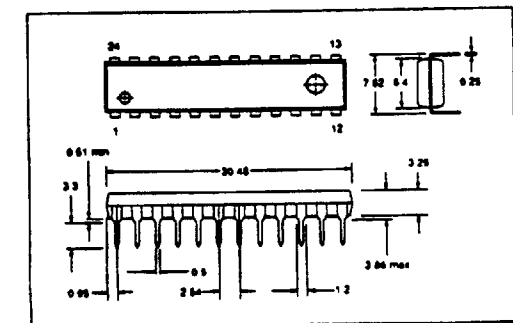
**3072-DIP24NS (LC3517A/AL)**



**3045B-MFP24 (LC3517A/AML)**



**3092-DIP24SNS 300 mil (LC3517AS/ASL)**

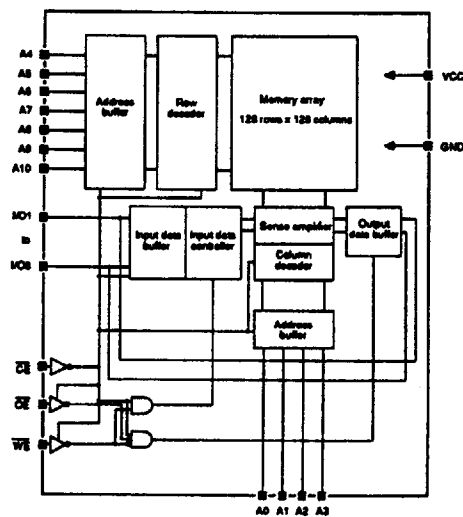


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BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1 to 8, 19, 22, 23	A0 to A10	Address inputs
9 to 11, 13 to 17	I/O1 to I/O6	Data inputs/outputs
12	GND	Ground
18	$\overline{CE}$	Chip enable input
20	$\overline{OE}$	Output enable input
21	$\overline{WE}$	Read/write select input
24	VCC	5 V supply

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	$V_{CC \max}$	7.0	V
Input voltage range	$V_{IH}$	-0.5 to $V_{CC} + 0.5$	V
Input/output voltage range	$V_{IO}$	-0.5 to $V_{CC} + 0.5$	V
Operating temperature range	$T_{OP}$	-30 to 85	deg. C
Storage temperature range	$T_{ST}$	-55 to 125	deg. C

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## Recommended Operating Conditions

 $T_a = 25 \text{ deg. C}$ 

Parameter	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	5.0	V
Supply voltage range	$V_{CC \text{ op}}$	4.5 to 5.5	V

## Electrical Characteristics

 $V_{CC} = 5 \text{ V} \pm 10\%$ ,  $T_a = -30 \text{ to } 85 \text{ deg. C}$  unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit	
			min	typ	max		
Quiescent supply current	$I_{CCQ1}$	$V_{CE} = 0 \text{ V}$ , $V_{IN} = V_{CC}$ or GND, $I_{VO} = 0 \text{ mA}$	-	30	55	mA	
		$V_{CE} = V_{IL}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{VO} = 0 \text{ mA}$	-	40	70		
Average supply current	$I_{CCA2}$	Minimum cycle time, duty = 100%, $I_{VO} = 0 \text{ mA}$	-	50	80	mA	
Standby supply current	$I_{CCS}$	$V_{CE} = V_{CC} - 0.2 \text{ V}$ , $V_{IN} = 0 \text{ V to } V_{CC}$ . See note 1.	$T_a = 60 \text{ deg. C}$	-	-	5.0	$\mu\text{A}$
			$T_a = 85 \text{ deg. C}$	-	-	30	
		$V_{CE} = V_{CC} - 0.2 \text{ V}$ , $V_{IN} = 0 \text{ V to } V_{CC}$ . See note 2.	$T_a = 25 \text{ deg. C}$	-	-	0.2	
			$T_a = 60 \text{ deg. C}$	-	-	1.0	
		$V_{CE} = V_{IH}$ , $V_{IN} = 0 \text{ V to } V_{CC}$	-	1.0	3.0	mA	
LOW-level input voltage	$V_{IL}$		-0.3	-	0.8	V	
HIGH-level input voltage	$V_{IH}$		2.2	-	$V_{CC} + 0.3$	V	
LOW-level output voltage	$V_{OL}$	$I_{OL} = 2.0 \text{ mA}$	-	-	0.4	V	
HIGH-level output voltage	$V_{OH}$	$I_{OH} = -1.0 \text{ mA}$	2.4	-	-	V	
Input capacitance	$C_{IN}$	$V_{IN} = 0 \text{ V}$ , $f = 1 \text{ MHz}$ , $T_a = 25 \text{ deg. C}$	-	-	5	pF	
Input/output capacitance	$C_{VO}$	$V_{VO} = 0 \text{ V}$ , $f = 1 \text{ MHz}$ , $T_a = 25 \text{ deg. C}$	-	-	10	pF	
Input leakage current	$I_{LI}$	$V_{IN} = 0 \text{ to } V_{CC}$	-1.0	-	1.0	$\mu\text{A}$	
Input/output leakage current	$I_{LO}$	$V_{CE}$ or $V_{BE} = V_{IH}$ , $V_{VO} = 0 \text{ V to } V_{CC}$	-5.0	-	5.0	$\mu\text{A}$	

## Notes

- LC3517A/AM/AS-10/12/15
- LC3517AL/AML/ASL-10/12/15
- Typical values are measured at  $V_{CC} = 5.0 \text{ V}$  and  $T_a = 25 \text{ deg. C}$ .

## Timing Characteristics

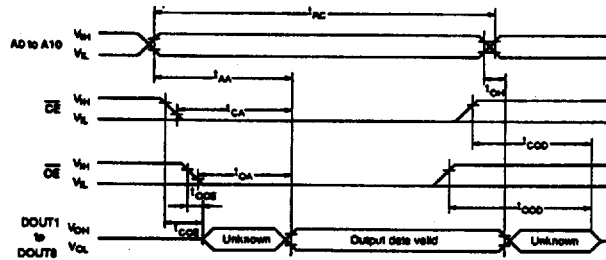
## Test conditions

- LOW-level pulse—0.6 V
- HIGH-level pulse—2.4 V
- Input rise and fall times—5 ns
- LOW-level timing reference— $V_{IL} = V_{OL} = 0.8 \text{ V}$
- HIGH-level timing reference— $V_{IH} = V_{OH} = 2.2 \text{ V}$
- Output load—1 TTL gate +  $C_L = 100 \text{ pF}$  (including jig capacitance)

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Read timing

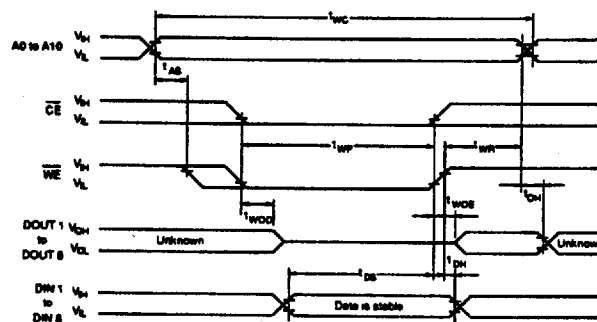


$V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_c = -30$  to  $85$  deg. C

Parameter	Symbol	LC3517A/AM/AS-10, LC3517AL/AML/ASL-10		LC3517A/AM/AS-12, LC3517AL/AML/ASL-12		LC3517A/AM/AS-15, LC3517AL/AML/ASL-15		Unit
		min	max	min	max	min	max	
Read cycle time	$t_{AC}$	100	-	120	-	150	-	ns
Address access time	$t_{AA}$	-	100	-	120	-	150	ns
Output-enable access time	$t_{OA}$	-	60	-	70	-	80	ns
Chip-enable access time	$t_{CA}$	-	100	-	120	-	150	ns
Output hold time	$t_{OH}$	5	-	5	-	5	-	ns
Output-enable propagation delay	$t_{OPE}$	5	-	5	-	5	-	ns
Chip-enable propagation delay	$t_{OPE}$	5	-	5	-	10	-	ns
Output-disable propagation delay	$t_{OOD}$	-	35	-	40	-	50	ns
Chip-disable propagation delay	$t_{COD}$	-	35	-	40	-	50	ns

Write timing

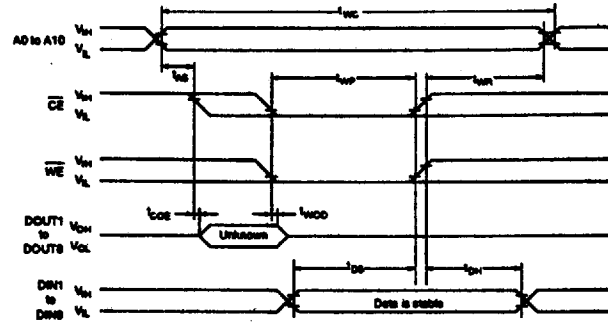
Write cycle 1



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Write cycle 2



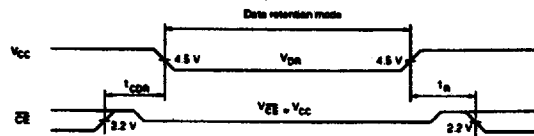
V<sub>CC</sub> = 5 V ±10%, T<sub>a</sub> = -30 to 85 deg. C

Parameter	Symbol	LC3517A/AMAS-10, LC3517AL/AML/ASL-10		LC3517A/AMAS-12, LC3517AL/AML/ASL-12		LC3517A/AMAS-15, LC3517AL/AML/ASL-15		Unit
		min	max	min	max	min	max	
Write cycle time	t <sub>bc</sub>	100	-	120	-	150	-	ns
Address setup time	t <sub>bs</sub>	0	-	0	-	0	-	ns
Write pulsewidth	t <sub>wp</sub>	75	-	95	-	120	-	ns
Write recovery time	t <sub>wr</sub>	10	-	10	-	10	-	ns
Data setup time	t <sub>ds</sub>	50	-	60	-	70	-	ns
Data hold time	t <sub>dh</sub>	0	-	0	-	0	-	ns
Write-enable propagation delay	t <sub>wce</sub>	5	-	5	-	5	-	ns
Write-disable propagation delay	t <sub>wod</sub>	-	35	-	40	-	50	ns

Notes

1. Hold WE HIGH during the read cycle.
2. Do not apply opposite phase signals to DOUT when it is connected to the output bus.
3. t<sub>wp</sub> can be measured when CE and WE are LOW.
4. t<sub>wr</sub>, t<sub>bs</sub> and t<sub>dh</sub> are measured from the time when CE or WE goes HIGH.
5. DOUT becomes high impedance after either CE or OE goes HIGH, or WE goes LOW.
6. t<sub>bs</sub> can be measured when CE and WE go LOW.
7. DOUT is high impedance when OE is HIGH during the write cycle.
8. DOUT has the same phase as the data to be written during the write cycle.
9. DOUT holds the data readout from the next address.

Data Retention Characteristics



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T<sub>a</sub> = -30 to 85 deg. C

Parameter	Symbol	Condition	Rating			Unit	
			min	typ	max		
Data retention mode supply voltage	V <sub>DR</sub>	V <sub>CE</sub> = V <sub>CC</sub> , V <sub>IN</sub> = 0 V to V <sub>CC</sub>	2.0	-	5.5	V	
Data retention mode supply current	I <sub>CCDR</sub>	V <sub>CE</sub> = V <sub>CC</sub> , V <sub>CC</sub> = 3.0 V, V <sub>IN</sub> = 0 V to V <sub>CC</sub> . See note 1.	T <sub>a</sub> = 60 deg. C	-	-	4.0	μA
			T <sub>a</sub> = 85 deg. C	-	-	20	
		V <sub>CE</sub> = V <sub>CC</sub> , V <sub>CC</sub> = 3.0 V, V <sub>IN</sub> = 0 V to V <sub>CC</sub> . See note 2.	T <sub>a</sub> = 25 deg. C	-	-	0.2	
			T <sub>a</sub> = 60 deg. C	-	-	1.0	
Chip-enable setup time	t <sub>CS</sub>		0	-	-	ns	
Chip-enable hold time	t <sub>H</sub>		t <sub>CH</sub>	-	-	ns	

Notes

1. LC3517A/AM/AS-10/12/15
2. LC3517AL/AML/ASL-10/12/15

Mode Selection

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Input/output	Supply current
Reset cycle	L	L	H	Data output	I <sub>CCA</sub>
Write cycle	L	X	L	Data input	I <sub>CCA</sub>
Output disable	L	H	X	High impedance	I <sub>CCA</sub>
Standby	H	X	X	High impedance	I <sub>CCS</sub>

Note

X = don't care

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