HD404720 Series

Description

The HD404720 Series is a 4-bit single-chip microcomputer which incorporare five timers, two serial interfaces, an A/D converter, an input capture timer, and an output compare timer. It also includes a 32.768-kHz oscillator and low-power dissipation modes. The HD404720 Series includes five chips: the HD404728 with 8-kword ROM; the HD404729 and HD4074729 with 16-kword ROM and PROM, respectively; the HD404720 and HD4074720 (modifications of the HD404729 and HD4074729) which also include an 8-kword pattern ROM.

The HD4074729 and HD4074720 are PROM versions (ZTAT™ microcomputers). A program can be written to the PROM by a PROM writer, which can dramatically shorten system development periods and smooth the process from debugging to mass production. (ZTAT™ versions are 27256-compatible.)

Features

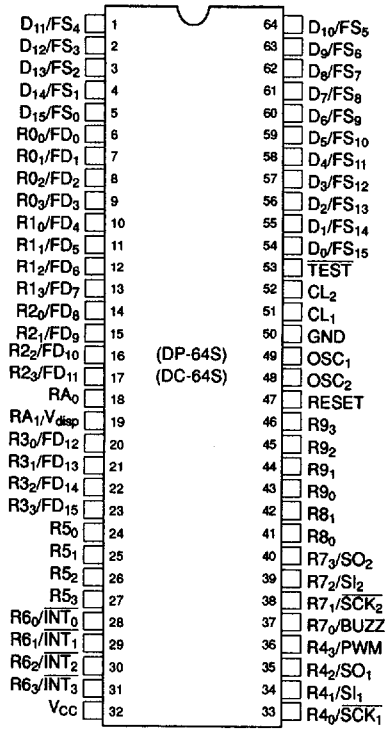
- 8,192-word × 10-bit program ROM (HD404728)
  16,384-word × 10-bit program ROM (HD404729, HD404720, HD4074729, HD4074720)
- 8,192-word × 10-bit pattern ROM (HD404720, HD4074720)
- 576-digit × 4-bit RAM (including 64-digit display RAM)
- 56 I/O pins including 32 high-voltage (40 V max.), high-current (15 mA max.) pins
- Three timer/counters
- Two-channel 8- or 16-bit clock-synchronous serial interface
- 14-bit PWM
- Ten interrupt sources
  - — Four by external sources, including two double-edge type sources
  - — Six by internal sources
- Subroutine stack up to 16 levels, including interrupts
- Four low-power dissipation modes
  - — Subactive mode
  - — Standby mode
  - — Watch mode
  - — Stop mode
- Built-in oscillator
  - — Crystal or ceramic ocsillator (an external clock is also possible)
  - — 32.768 kHz-crystal subclock
- Instruction cycle time: 0.89 to 10 μs

Ordering Information

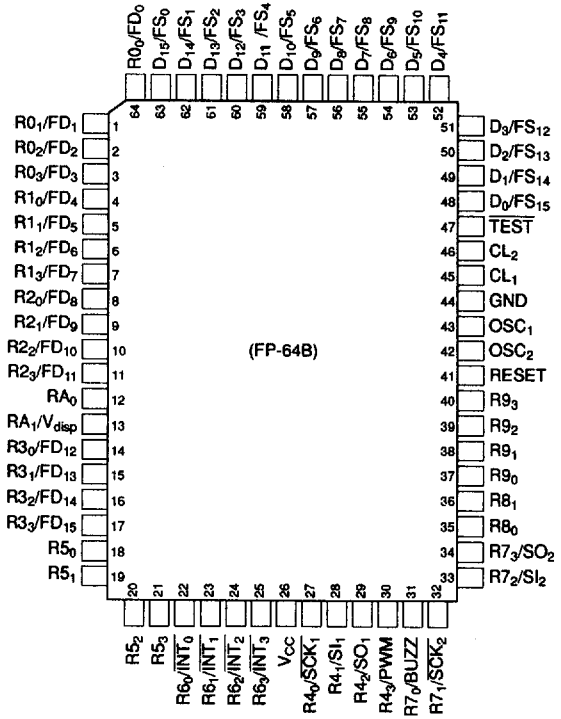
Type	Product Name	Model Name	Program ROM (Words)	Pattern ROM (Words)	Package
Mask ROM	HD404728	HD404728S	8,192	—	64 pin plastic shrink DIP (DP-64S)
		HD404728FS			64 pin plastic QFP (FP-64B)
		HD404728H			64 pin plastic QFP (FP-64A)
	HD404729	HD404729S	16,384		64 pin plastic shrink DIP (DP-64S)
		HD404729FS			64 pin plastic QFP (FP-64B)
		HD404729H			64 pin plastic QFP (FP-64A)
	HD404720	HD404720S		8,192	64 pin plastic shrink DIP (DP-64S)
		HD404720FS			64 pin plastic QFP (FP-64B)
ZTAT™	HD4074729	HD4074729S	16,384	—	64 pin plastic shrink DIP (DP-64S)
		HD4074729FS			64 pin plastic QFP (FP-64B)
		HD4074729H			64 pin plastic QFP (FP-64A)
		HD4074729C*			64 pin ceramic shrink DIP (window) (DC-64S*)
	HD4074720	HD4074720S		8,192	64 pin plastic shrink DIP (DP-64S)
		HD4074720FS			64 pin plastic QFP (FP-64B)
		HD4074720C*			64 pin ceramic shrink DIP (window) (DC-64S*)

Note: * Available as a sample.

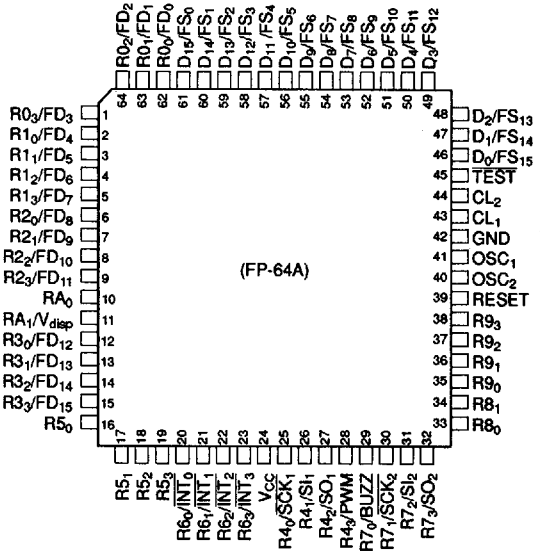
Pin Arrangement



(top view)



(top view)



(top view)

Pin Description

Pin Number					Pin Number				
DP-64S DC-64S	FP-64B	FP-64A	Pin Name	Input/ Output	DP-64S DC-64S	FP-64B	FP-64A	Pin Name	Input/ Output
1	59	57	D_{11}/FS_4	I/O	33	27	25	$R4_0/\overline{SCK_1}$	I/O
2	60	58	D_{12}/FS_3	I/O	34	28	26	$R4_1/SI_1$	I/O
3	61	59	D_{13}/FS_2	I/O	35	29	27	$R4_2/SO_1$	I/O
4	62	60	D_{14}/FS_1	I/O	36	30	28	$R4_3$/PWM	I/O
5	63	61	D_{15}/FS_0	I/O	37	31	29	$R7_0$/BUZZ	I/O
6	64	62	$R0_0/FD_0$	I/O	38	32	30	$R7_1/\overline{SCK_2}$	I/O
7	1	63	$R0_1/FD_1$	I/O	39	33	31	$R7_2/SI_2$	I/O
8	2	64	$R0_2/FD_2$	I/O	40	34	32	$R7_3/SO_2$	I/O
9	3	1	$R0_3/FD_3$	I/O	41	35	33	$R8_0$	I/O
10	4	2	$R1_0/FD_4$	I/O	42	36	34	$R8_1$	I/O
11	5	3	$R1_1/FD_5$	I/O	43	37	35	$R9_0$	I
12	6	4	$R1_2/FD_6$	I/O	44	38	36	$R9_1$	I
13	7	5	$R1_3/FD_7$	I/O	45	39	37	$R9_2$	I
14	8	6	$R2_0/FD_8$	I/O	46	40	38	$R9_3$	I
15	9	7	$R2_1/FD_9$	I/O	47	41	39	RESET	I
16	10	8	$R2_2/FD_{10}$	I/O	48	42	40	OSC_2	O
17	11	9	$R2_3/FD_{11}$	I/O	49	43	41	OSC_1	I
18	12	10	RA_0	I	50	44	42	GND	
19	13	11	RA_1/V_{disp}	I	51	45	43	CL_1	I
20	14	12	$R3_0/FD_{12}$	I/O	52	46	44	CL_2	O
21	15	13	$R3_1/FD_{13}$	I/O	53	47	45	$\overline{TEST}$	I
22	16	14	$R3_2/FD_{14}$	I/O	54	48	46	D_0/FS_{15}	I/O
23	17	15	$R3_3/FD_{15}$	I/O	55	49	47	D_1/FS_{14}	I/O
24	18	16	$R5_0$	I/O	56	50	48	D_2/FS_{13}	I/O
25	19	17	$R5_1$	I/O	57	51	49	D_3/FS_{12}	I/O
26	20	18	$R5_2$	I/O	58	52	50	D_4/FS_{11}	I/O
27	21	19	$R5_3$	I/O	59	53	51	D_5/FS_{10}	I/O
28	22	20	$R6_0/\overline{INT_0}$	I/O	60	54	52	D_6/FS_9	I/O
29	23	21	$R6_1/\overline{INT_1}$	I/O	61	55	53	D_7/FS_8	I/O
30	24	22	$R6_2/\overline{INT_2}$	I/O	62	56	54	D_8/FS_7	I/O
31	25	23	$R6_3/\overline{INT_3}$	I/O	63	57	55	D_9/FS_6	I/O
32	26	24	V_{CC}		64	58	56	D_{10}/FS_5	I/O

Pin Functions

Power Supply

V_{CC}: Apply the power voltage to this pin.

GND: Connect to ground.

$\overline{TEST}$: Used for test purposes only. Connect it to V_{CC}.

RESET: Resets the MCU.

Oscillators

OSC_1, OSC_2: Used as pins for the internal oscillator circuit. They can be connected to a crystal resonator or a ceramic resonator, or OSC_1 can be connected to an external oscillator circuit.

CL_1, CL_2: Used for a 32.768-kHz crystal oscillator that acts as a clock.

Ports

D_0–D_{15} (D Port): Input/output port addressable by individual bits. Each port output consists of an open-drain PMOS which enables high-voltage, high-current drive ability for its pin. These pins are multiplexed with the segment pins used for the VFD controller.

R0–RA (R Ports): Input/output ports addressable in 4-bit units, except for R8 and RA which are addressable by 2 bits. R9 and RA are input-only ports and R0 to R8 are input/output ports. The R4 to R9 port pins are standard pins, but the R0 to R3 and RA pins are high-voltage pins. Each of the R0 to R3 output pins consists of an open-drain PMOS which enables high-voltage, high-current drive ability for its pin. These pins are multiplexed with the digit pins for the VFD controller. Port pins $R4_0$ to $R4_3$, $R6_0$ to $R6_3$, and $R7_0$ to $R7_3$ are multiplexed with peripheral pins.

Interrupts

$\overline{INT_0}$, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{INT_3}$: External input interrupts to the MCU. $\overline{INT_1}$ is also used as an external event input for timer B. $\overline{INT_0}$ to $\overline{INT_3}$ are multiplexed with $R6_0$ to $R6_3$, respectively.

Serial Interface

$\overline{SCK_1}$, $\overline{SCK_2}$: Input/output serial interface clock pins that are multiplexed with pins $R4_0$ and $R7_1$, respectively.

SI_1, SI_2: Serial interface receive data input pins that are multiplexed with pins $R4_1$ and $R7_2$, respectively.

SO_1, SO_2: Serial interface transmit data output pins that are multiplexed with pins $R4_2$ and $R7_3$, respectively.

Timer

BUZZ: Outputs a variable-duty square wave. It is multiplexed with $R7_0$.

VFD Controller

FD_0–FD_{15}: Digit pins for the vacuum fluorescent display (VFD) controller. They are multiplexed with port pins $R0_0$ to $R3_3$.

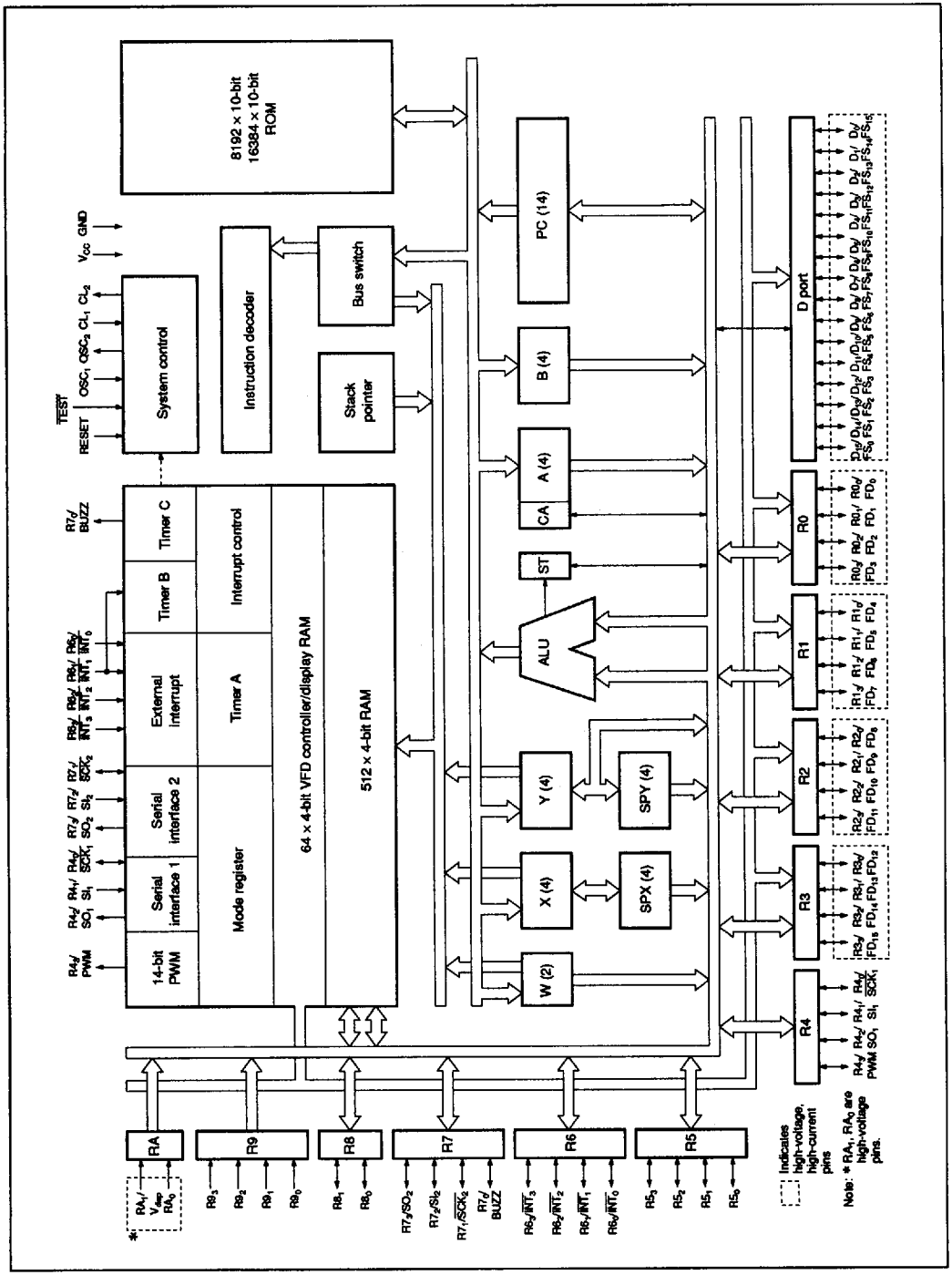
FS_0–FS_{15}: Segment pins for the VFD controller. They are multiplexed with the D port pins.

PWM

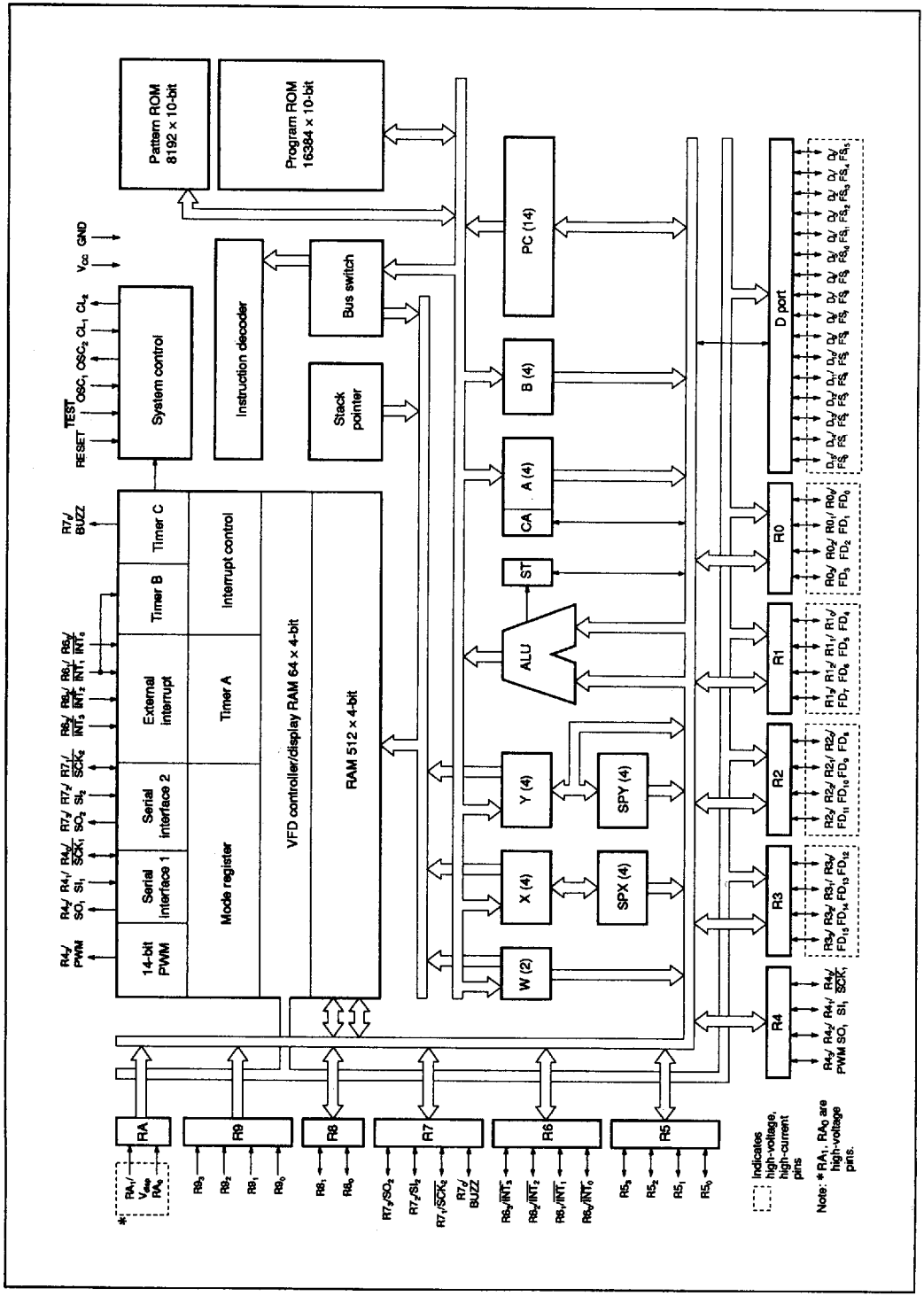
PWM: Outputs a square wave from the PWM. It is multiplexed with $R4_3$.

Block Diagram

1. HD404728, HD404729, HD4074729



2. HD404720, HD4074720



Memory Map

Program ROM Memory Map

The program ROM memory map is shown in figure 1, and the ROM is described in detail below.

Vector Address Area ($0000–$000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines. After a MCU reset or interrupt execution, the program starts from the vector address.

Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to the subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF):

- HD404728, HD404729, HD4074729: Reserved for ROM data that is referenced as a pattern by the P instruction.
- HD404720, HD4074720: Reserved for ROM data that can be referenced as a pattern by the P instruction. The data in this area is available when bit 1 of the pattern bank register (PBNK) is 0.

Program Area:
$0000–$1FFF (HD404728)
$0000–$3FFF (HD404729, HD404720, HD4074729, HD4074720)

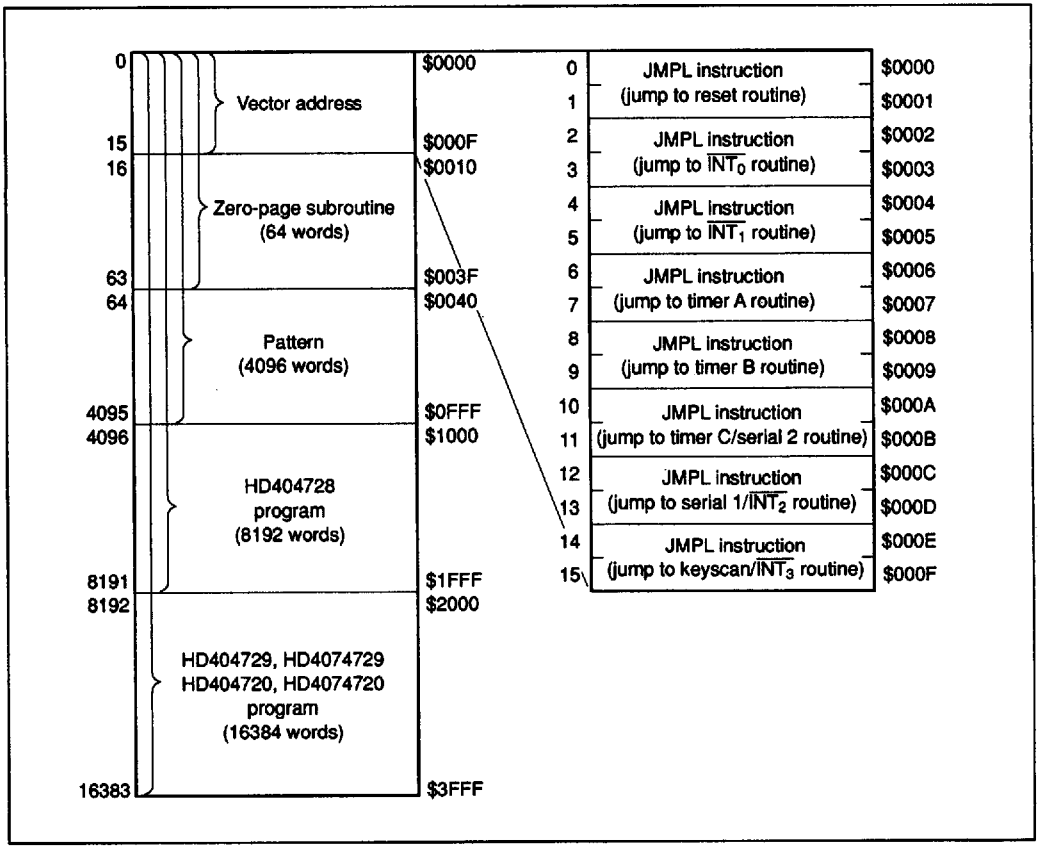


Figure 1 ROM Memory Map

Pattern ROM Memory Map (HD404720, HD4074720)

The pattern ROM memory map is shown in figure 2. The access conditions are shown in figures 3 to 5 and described below.

8-kword Pattern Area ($0000–$1FFF): Data in this area is accessed as the pattern data of the P instruction, when bit 1 of PBNK (pattern ROM bank register) is 1. When bit 0 of PBNK (PBNK0) is 0, area $0000–$0FFF is accessed, and when PBNK0 = 1, area $1000–$1FFF is accessed.

When PBNK1 = 0, data in the area limited to $0000–$0FFF in the 16-kword program area is accessed as the pattern data of the P instruction.

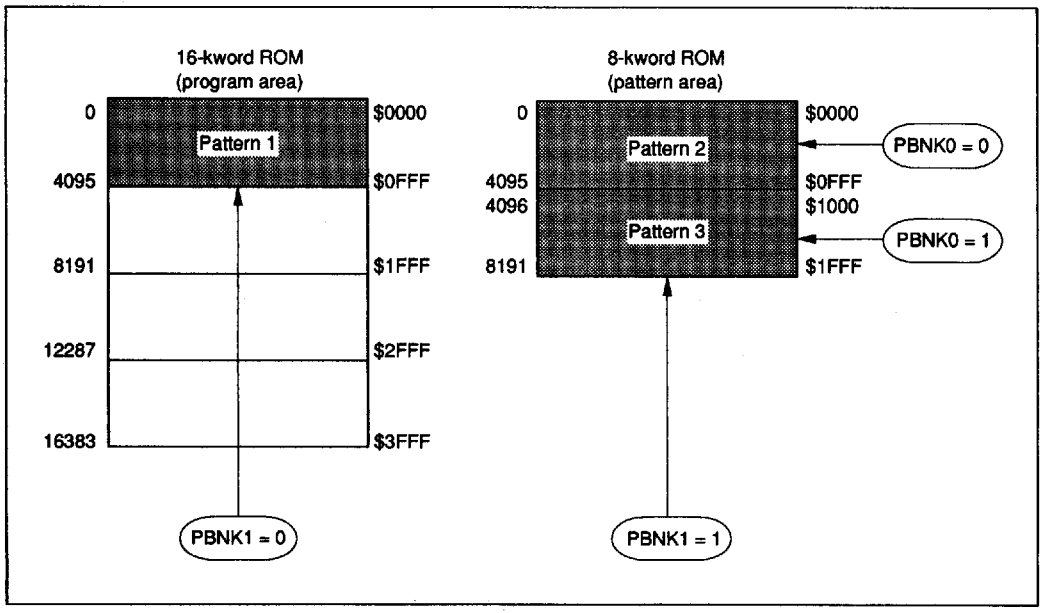
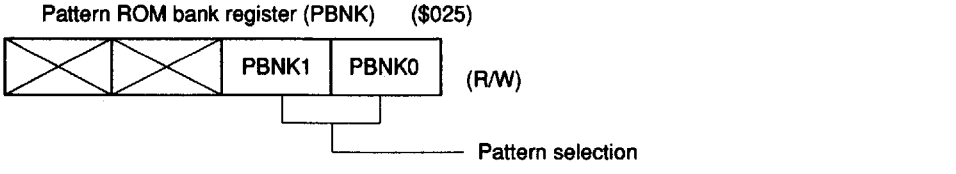


Figure 2 Pattern Reference Area of the P Instruction



PBNK1	PBNK0	Pattern
0	*	Pattern 1
1	0	Pattern 2
1	1	Pattern 3

Note: At reset, PBNK1 = 0 and PBNK0 = 0.

Figure 3 Pattern ROM Bank Register

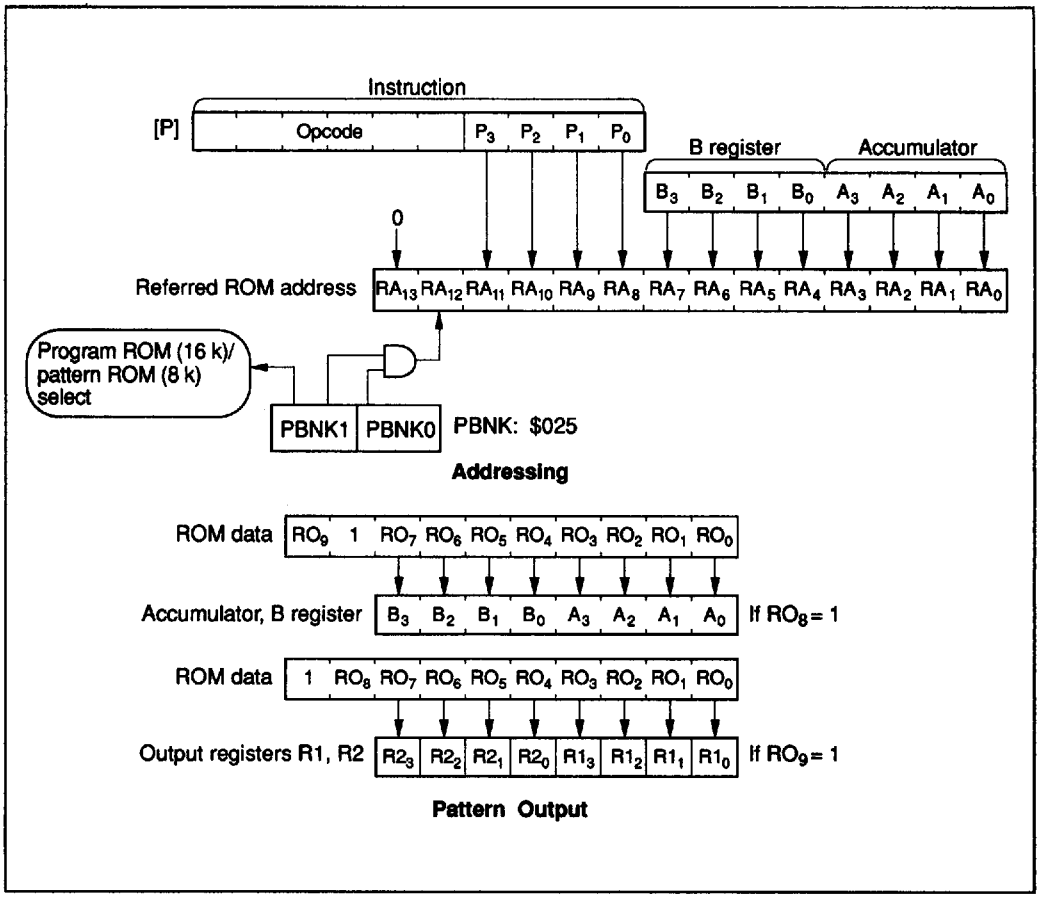


Figure 4 P (Pattern) Instruction

Notes for Pattern ROM Bank Control:

- Case 1: When changing PBNK data during an interrupt routine or subroutine, the previous PBNK data must be stored in RAM and retrieved just before the RTN or RTNI instruction.
- Case 2: In some cases, the PBNK set operation must be programmed just before the BR, TBR, BRL, or JMPL instruction.

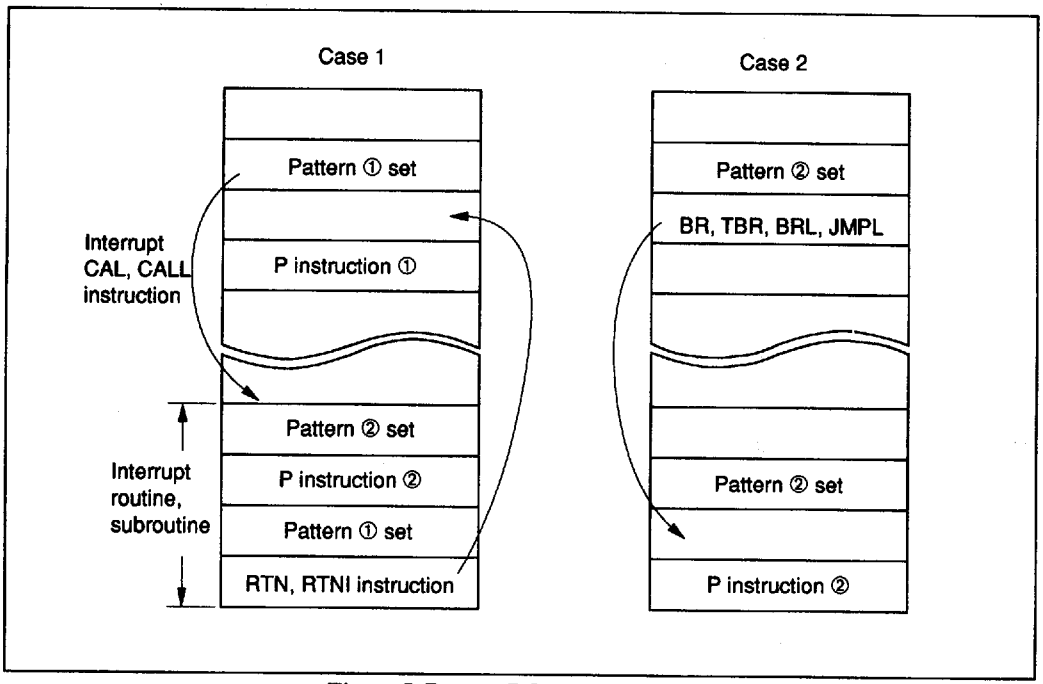


Figure 5 Pattern ROM Bank Control

RAM Memory Map

The MCU contains a 512-digit × 4-bit RAM area for data and stack areas. In addition, interrupt control bits, special function registers, and a VFD data area are mapped onto the same RAM memory space outside this area. The RAM memory map is shown in figures 6-1 and 6-2, and the RAM area is described in detail below.

Interrupt Control Bits Area ($000–$003, $020–$023): Used for interrupt control (figure 7). It can be accessed only by RAM bit manipulation instructions. However, note that the interrupt request flag cannot be set by software, the RSP bit is used only to reset the stack pointer, the LSON and WDON flags are accessed only by RAM bit manipulation instructions, and the WDON flag can only be set to 1 by the SEM and SEMD instructions.

Special Function Registers Area ($004–$01F, $024–$03F): Used as mode registers for external interrupts, the serial interface, the timer/counters, and as data control registers and data registers for I/O ports. As shown in figure 6, there are three types of registers: read-only, write-only, and read/write. These registers cannot be used by RAM bit manipulation instructions.

VFD Data Area ($060–$09F): Used for storing VFD data which is automatically output to the segment pins as display data. Data 1 turns on a light; data 0 turns it off.

Data Area ($040–$04F, $0A0–$24F): The memory registers (MR), which are within 16 digits ($040–$04F), can also be accessed by the LAMR and XMRA instructions (figure 8).

Stack Area ($3C0–$3FF): Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine call (CAL or CALL instruction) and interrupts. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. The stack area and data to be saved in it are shown in figure 8.

The program counter is popped from the stack by the RTN and RTNI instructions, but the status and carry flags can only be popped from the stack by the RTNI instruction. Any unused area is available for data storage.

HD404728, HD404729, HD4074729

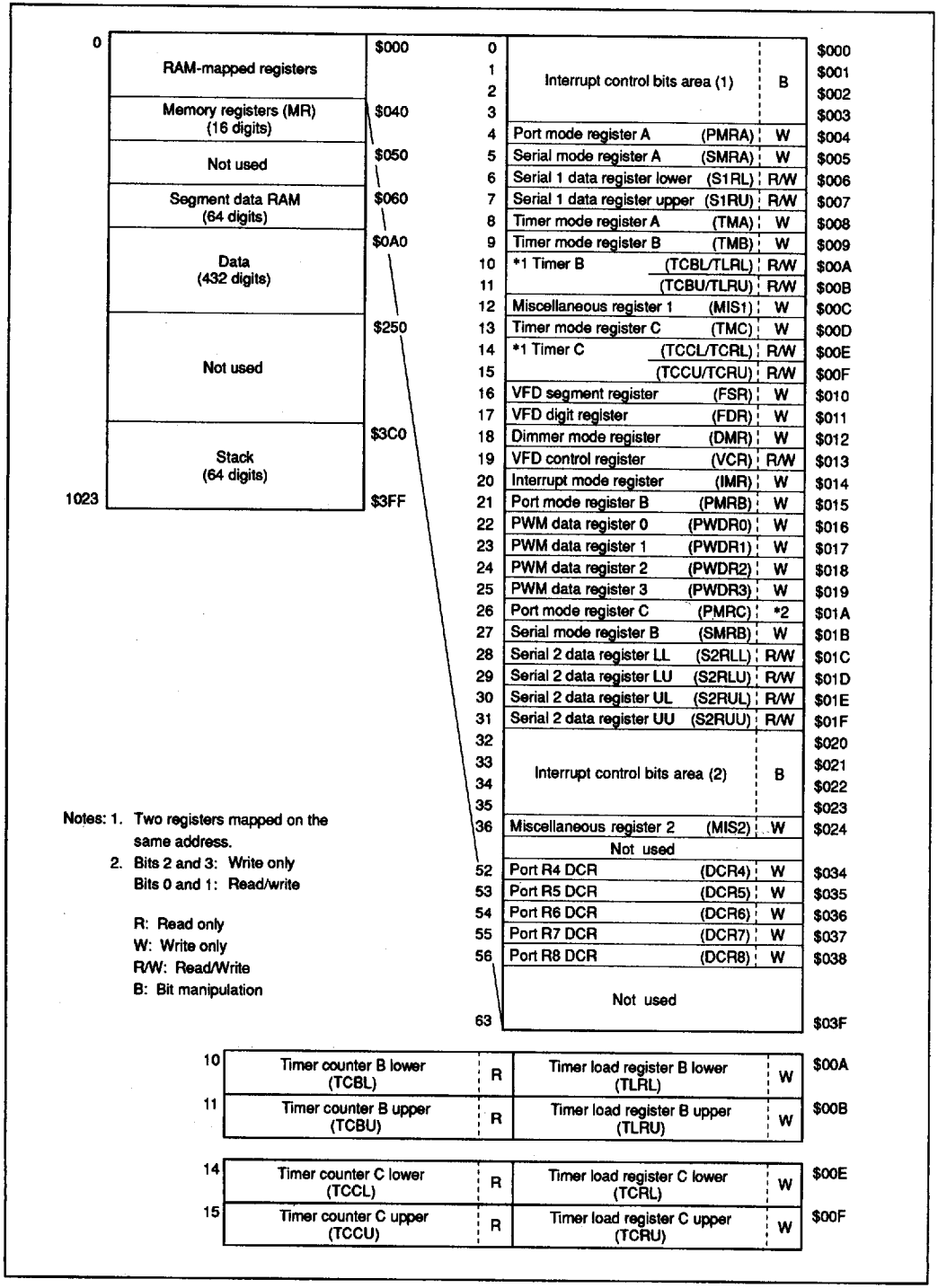


Figure 6-1 RAM Memory Map (HD404728, HD404729, HD4074729)

HD404720, HD4074720

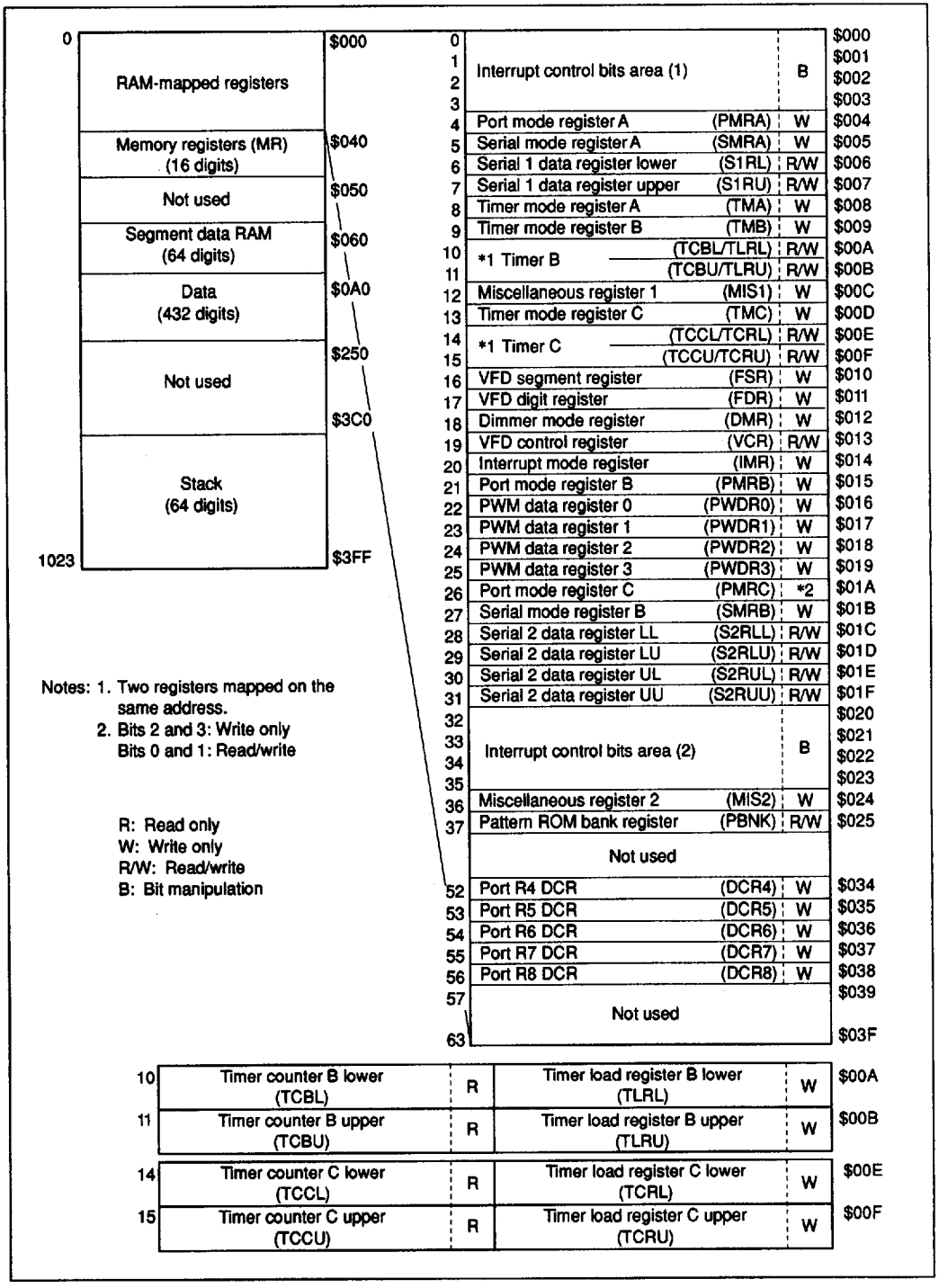


Figure 6-2 RAM Memory Map (HD404720, HD4074720)

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	IMTC (IM of timer C)	IFTC (IF of timer C)	IMTB (IM of timer B)	IFTB (IF of timer B)	$002
3	IMKS (IM of keyscan)	IFKS (IF of keyscan)	IMS1 (IM of serial 1)	IFS1 (IF of serial 1)	$003
32			WDON (Watchdog on flag)	LSON (Low speed on flag)	$020
33			Reserved		$021
34	IMS2 (IM of serial 2)	IFS2 (IF of serial 2)			$022
35	IM3 (IM of $\overline{INT_3}$)	IF3 (IF of $\overline{INT_3}$)	IM2 (IM of $\overline{INT_2}$)	IF2 (IF of $\overline{INT_2}$)	$023

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Note: Bits in the interrupt control bits area and register flag area are set by the SEM or SEMD instruction, reset by the REM or REMD instruction, and tested by the TM or TMD instruction. Other instructions have no effect.
However, note that the IF cannot be set by the SEM or SEMD instruction. If the RSP bit or a non-existent bit is tested by the TM or TMD instruction, its status is undefined.
The WDON flag can only be used by the SEM or SEMD instruction (it is reset only by MCU reset).

Figure 7 Configuration of Interrupt Control Bits and Register Flag Areas

Memory registers			Stack area		
64	MR (0)	$040	960 Level 16		$3C0
65	MR (1)	$041	Level 15		
66	MR (2)	$042	Level 14		
67	MR (3)	$043	Level 13		
68	MR (4)	$044	Level 12		
69	MR (5)	$045	Level 11		
70	MR (6)	$046	Level 10		
71	MR (7)	$047	Level 9		
72	MR (8)	$048	Level 8		
73	MR (9)	$049	Level 7		
74	MR (10)	$04A	Level 6		
75	MR (11)	$04B	Level 5		
76	MR (12)	$04C	Level 4		
77	MR (13)	$04D	Level 3		
78	MR (14)	$04E	Level 2		
79	MR (15)	$04F	1023 Level 1		$3FF

	Bit 3	Bit 2	Bit 1	Bit 0	
1020	ST	$\overline{PC_{13}}$	$\overline{PC_{12}}$	$\overline{PC_{11}}$	$3FC
1021	$\overline{PC_{10}}$	$\overline{PC_9}$	$\overline{PC_8}$	$\overline{PC_7}$	$3FD
1022	CA	$\overline{PC_6}$	$\overline{PC_5}$	$\overline{PC_4}$	$3FE
1023	$\overline{PC_3}$	$\overline{PC_2}$	$\overline{PC_1}$	$\overline{PC_0}$	$3FF

PC_{13}–PC_0: Program counter
ST: Status flag
CA: Carry flag

Figure 8 Configuration of Memory Registers and Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are shown in figure 9 and described below.

Accumulator (A), B Register (B): Four-bit registers used to hold results from the arithmetic logic unit (ALU) and to transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): Four-bit registers used to supplement the X and Y registers.

Carry Flag (CA): One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is also affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt, and popped from the stack by the RTNI instruction—but not by the RTN instruction.

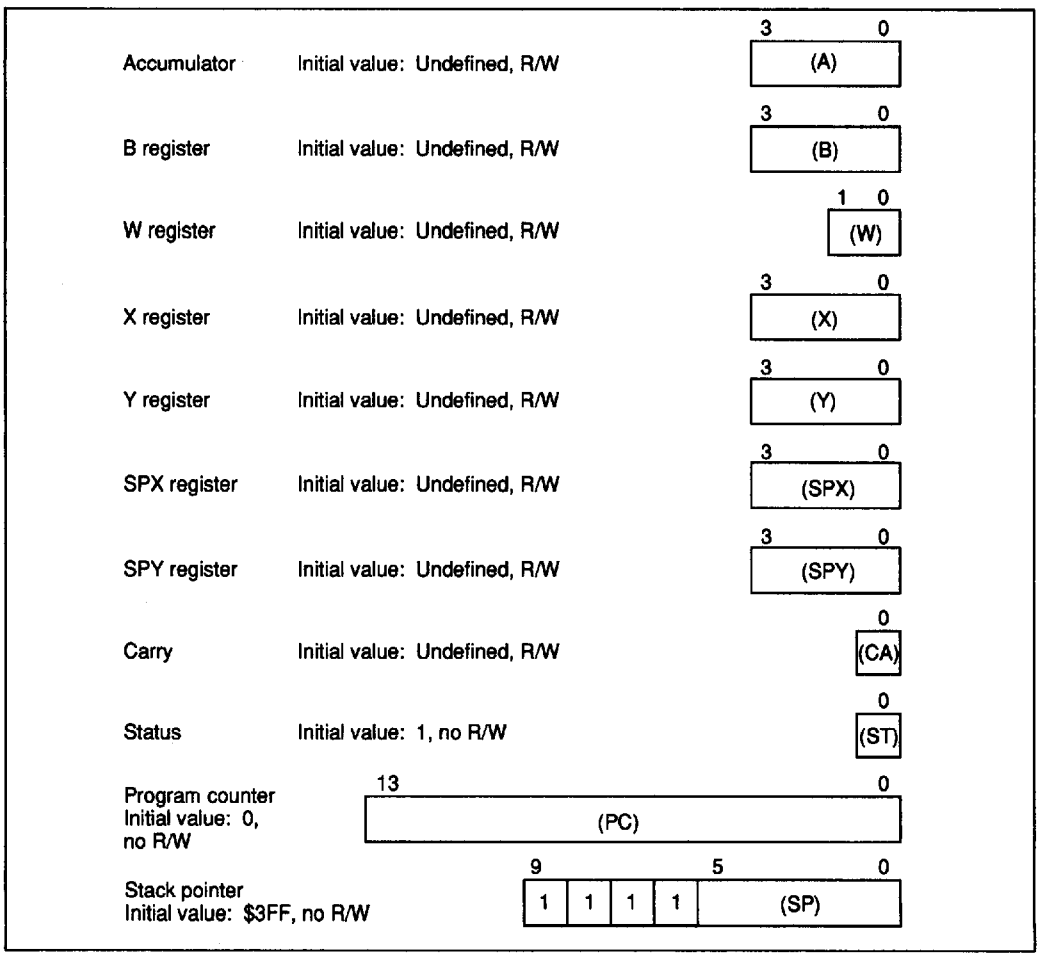


Figure 9 Registers and Flags

Status Flag (ST): One-bit flag that indicates an ALU overflow or ALU non-zero generated during an arithmetic or compare instruction, or the result of a bit test instruction. ST is used as a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after the BR, BRL, CAL, or CALL instruction is fetched, regardless of whether the instruction is executed or skipped. The contents of ST are pushed onto the stack during an interrupt, and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Program Counter (PC): A 14-bit counter that points to the ROM address of the instruction being executed.

Stack Pointer (SP): Ten-bit pointer that contains the address of the stack area to be used as the next level. The SP is initialized to $3FF by MCU reset. It is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped from the stack. Since the top 4 bits of the SP are fixed to 1111, a stack of up to 16 levels can be used.

The SP is initialized to $3FF in two ways: by MCU reset or by resetting the RSP bit with the REM or REMD instruction.

Reset

The MCU is reset by setting the RESET pin high. At power-on or when stop mode is cancelled, RESET must be high for at least one t_{RC} to enable the oscillator to stabilize. In other cases, a RESET input for two instruction cycles resets the MCU.

Initial values of the registers and counters after MCU reset are listed in table 1.

Note that the reset signal is not acknowledged by the MCU from power-on until the oscillation stabilizes (t_{RC}), so the statuses within the MCU and at the I/O pins are not defined.

Table 1 Initial Values After MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status flag		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
Interrupt flags/ mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	High-voltage port data register	(PDR)	All bits 0	Enables output at level 0
	Standard port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCR)	All bits 0	Turns output buffer off (to high impedance)
	Port mode register A	(PMRA)	0000	Refer to Port Mode Register A section
	Port mode register B	(PMRB)	0000	Refer to Port Mode Register B section
	Port mode register C	(PMRC)	0000	Refer to Port Mode Register C section
	Interrupt mode register	(IMR)	0000	Refer to Interrupt Mode Register section

Table 1 Initial Values After MCU Reset (cont)

Item		Abbr.	Initial Value	Contents
Timer/ counters, serial interface	Timer mode register A	(TMA)	0000	Refer to Timer Mode Register A section
	Timer mode register B	(TMB)	0000	Refer to Timer Mode Register B section
	Timer mode register C	(TMC)	0000	Refer to Timer Mode Register C section
	Serial mode register A	(SMRA)	0000	Refer to Serial Mode Register A section
	Serial mode register B	(SMRB)	0000	Refer to Serial Mode Register B section
	Prescaler S		$000	—
	Prescaler W		$00	—
	Timer counter A	(TCA)	$00	—
	Timer counter B	(TCB)	$00	—
	Timer counter C	(TCC)	$00	—
	Timer load register B	(TLR)	$00	—
	Timer load register C	(TCR)	$00	—
	Octal counter	(OC)	000	—
VFD	VFD segment register	(FSR)	0000	Refer to VFD Segment Register section
	VFD digit register	(FDR)	0000	Refer to VFD Digit Register section
	VFD dimmer mode register	(DMR)	0000	Refer to VFD Dimmer Mode Register section
	VFD control register	(VCR)	0000	Refer to VFD Control Register section
PWM	PWM data register	(PWDR)	$0000	Refer to PWM Data Register section
Bit register	Low speed on flag	(LSON)	0	Refer to Operating Modes section
	Watchdog timer on flag	(WDON)	0	Refer to Timer C section
Miscellaneous register 1		(MIS1)	0000	Refer to Miscellaneous Register 1 section
Miscellaneous register 2		(MIS2)	0000	Refer to Miscellaneous Register 2 section
Pattern ROM bank register*		(PBNK)	00	Refer to Pattern ROM section

Note: * Applies to HD404720 and HD4074720.
The status of other registers and flags after MCU reset are shown on next page.

Item	Abbr.	Status After Cancellation of Stop Mode by MCU Reset	In Other Cases at MCU Reset
Carry flag	(CA)	Pre-MCU-reset values are not guaranteed: values must be initialized by software	Pre-MCU-reset values are not guaranteed: values must be initialized by software
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
Serial 1 data register	(SR1)		
Serial 2 data register	(SR2)		
Miscellaneous register 2	(MIS2)		
RAM		Pre-MCU-reset (pre-STOP-instruction) values are retained	

Interrupts

The MCU has ten interrupt sources: four external signals ($\overline{INT_0}$–$\overline{INT_3}$), three timer/counters (timer A, timer B, and timer C), two serial interfaces (serial 1 and serial 2), and a key scan. An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (IE) controls the entire interrupt process.

Interrupt Control Bits and Interrupt Processing: Locations $000 through $003 and $020 through $023 in RAM are reserved for the interrupt control bits which can only be accessed by RAM bit manipulation instructions. The interrupt request flags (IFs) can only be set by signals from interrupt sources. MCU reset initializes the interrupt enable flag (IE) and interrupt request flags (IFs) to 0 and the interrupt masks (IMs) to 1.

A block diagram of the interrupt control circuit is shown in figure 10, interrupt priorities and vector addresses are listed in table 2, and the interrupt processing conditions for the ten interrupt sources are listed in table 3. An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the IE is 1 at that point, interrupt processing begins. A priority programmable logic array generates the vector address assigned to that interrupt source.

The interrupt processing sequence is shown in figure 11, and an interrupt processing flowchart is shown in figure 12. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry flag, status flag, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMPL instruction at each vector address to branch the program to the start address of the interrupt routine, and reset the IF by an instruction within the interrupt routine.

Note: The interrupt mask bit will not be set by interrupt processing.

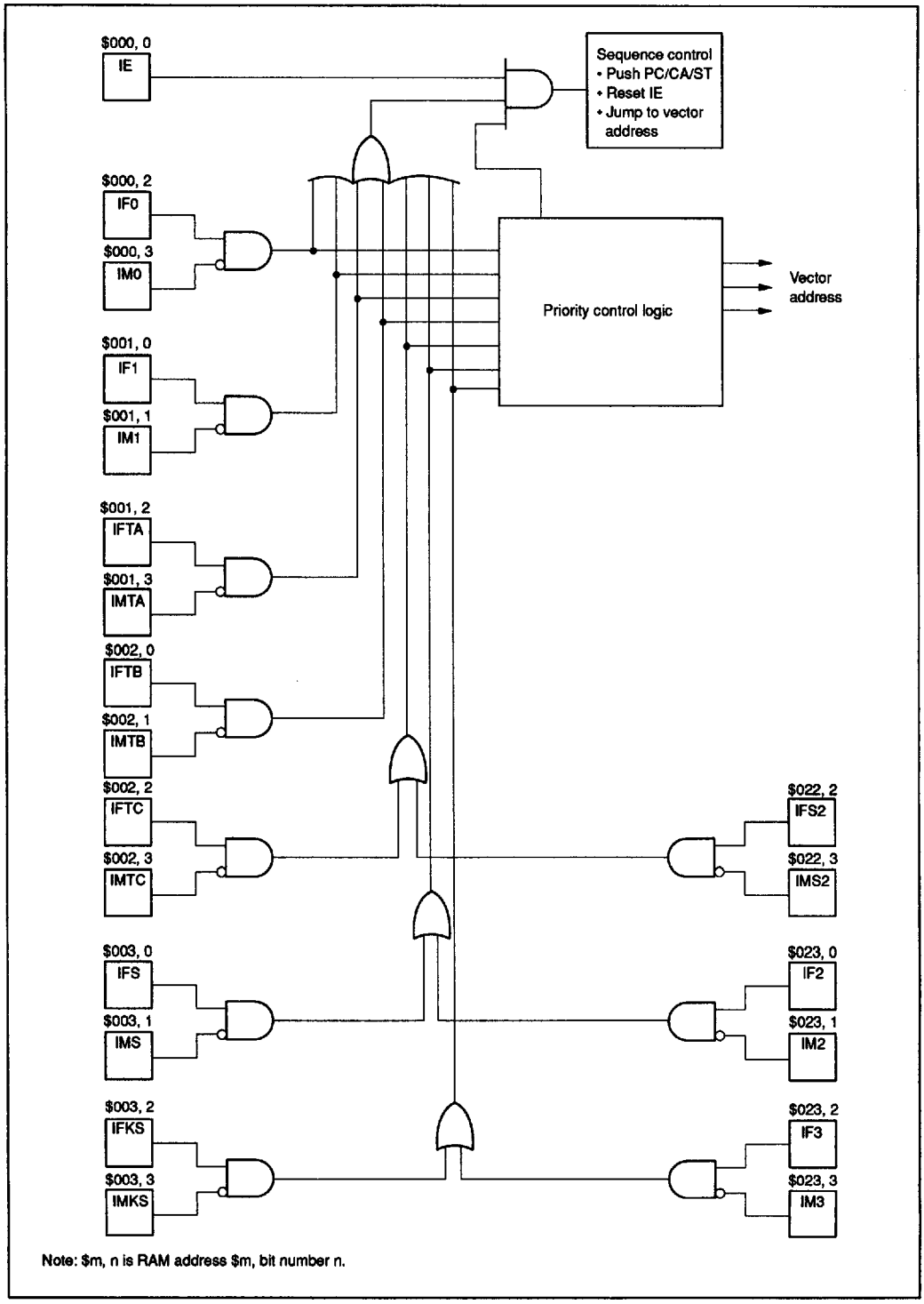


Figure 10 Block Diagram of Interrupt Control Circuit

Table 2 Vector Addresses and Interrupt Priorities

Reset/Interrupt	Priority	Vector Address
RESET	—	$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
Timer A	3	$0006
Timer B	4	$0008
Timer C, Serial 2	5	$000A
Serial 1, $\overline{INT_2}$	6	$000C
Key scan, $\overline{INT_3}$	7	$000E

Table 3 Interrupt Conditions

	Interrupt Source						
Interrupt Control Bit	$\overline{INT_0}$	$\overline{INT_1}$	Timer A	Timer B	Timer C, Serial 2	Serial 1, $\overline{INT_2}$	Key Scan, $\overline{INT_3}$
IE	1	1	1	1	1	1	1
IF0 • $\overline{IM0}$	1	0	0	0	0	0	0
IF1 • $\overline{IM1}$	*	1	0	0	0	0	0
IFTA • $\overline{IMTA}$	*	*	1	0	0	0	0
IFTB • $\overline{IMTB}$	*	*	*	1	0	0	0
IFTC • $\overline{IMTC}$ + IFS2 • $\overline{IMS2}$	*	*	*	*	1	0	0
IFS1 • $\overline{IMS1}$ + IF2 • $\overline{IM2}$	*	*	*	*	*	1	0
IFKS • $\overline{IMKS}$ + IF3 • $\overline{IM3}$	*	*	*	*	*	*	1

Note: Bits marked * can be either 0 or 1. Their values have no effect on operation.

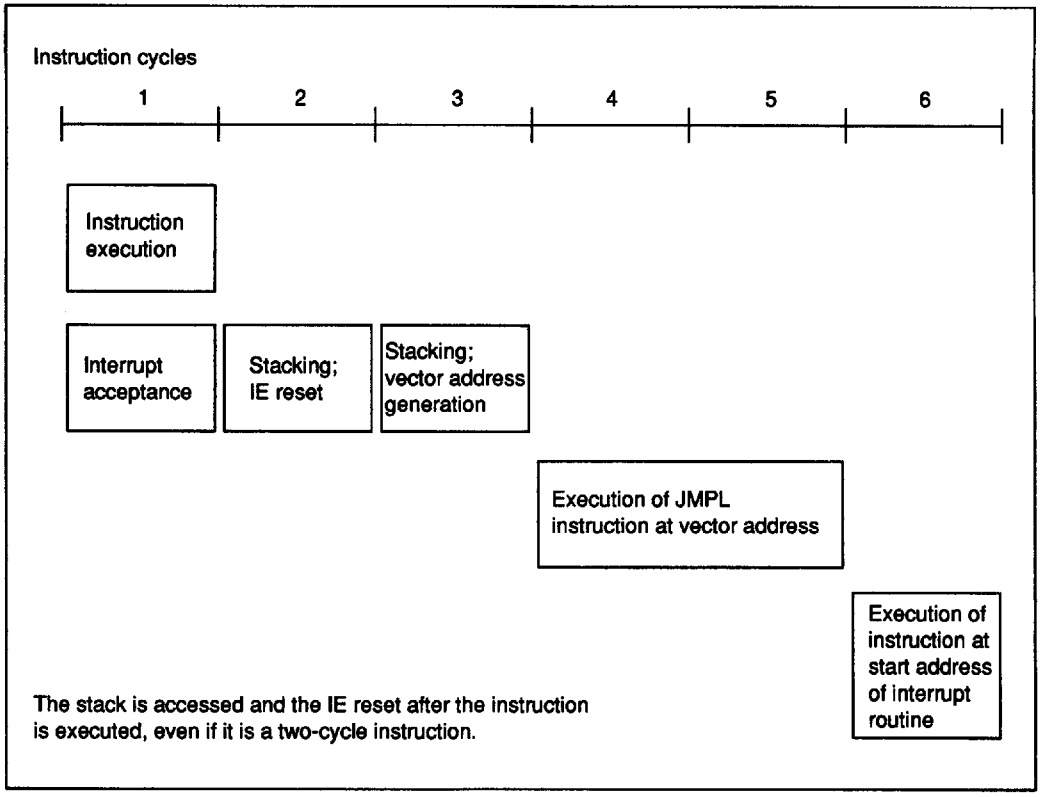


Figure 11 Interrupt Processing Sequence

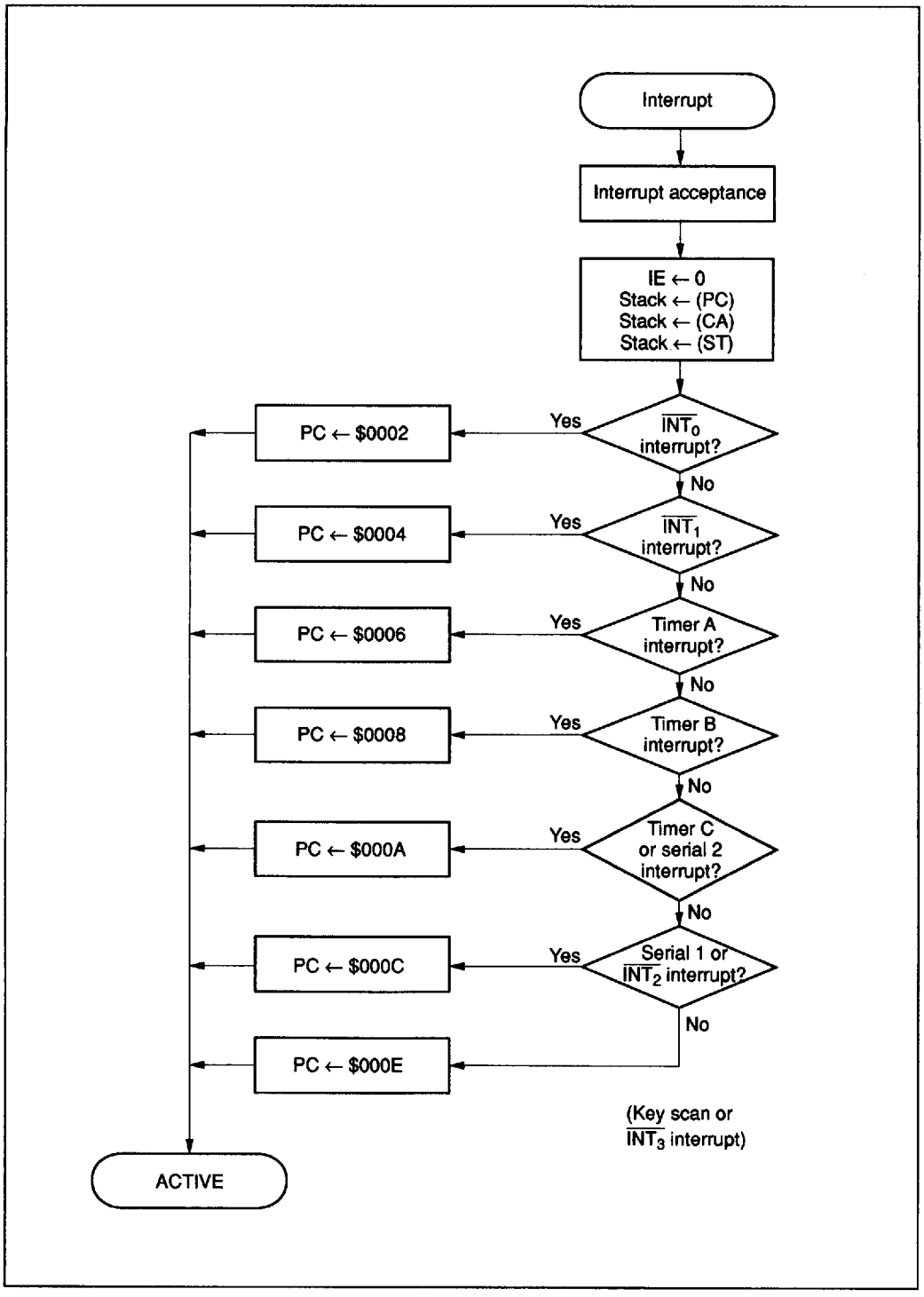


Figure 12 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): Controls all interrupts (table 4). IE is reset to 0 by an interrupt and set to 1 by the RTNI instruction.

External Interrupts ($\overline{INT_0}$–$\overline{INT_3}$): Specified by port mode registers A and B (PMRA: $004, PMRB: $015).

The $\overline{INT_1}$ input can be used as a clock input for timer B in which case timer B increments at each falling edge of the $\overline{INT_1}$ input. The external interrupt request flag (IM1) must be set to inhibit the $\overline{INT_1}$ interrupt request.

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0; IF2: $023, Bit 0; IF3: $023, Bit 2): Set at the rising or falling edges of the corresponding $\overline{INT_0}$ to $\overline{INT_3}$ inputs (table 5).

IF0 and IF1 are set at the falling edges of $\overline{INT_0}$ and $\overline{INT_1}$, respectively, and IF2 and IF3 are set at either the rising or falling edges of $\overline{INT_2}$ and $\overline{INT_3}$, respectively. The active edge is selected by the interrupt mode register (IMR: $014).

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1; IM2: $023, Bit 1; IM3: $023, Bit 3): Mask interrupt requests caused by the corresponding external interrupt request flags (table 6).

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): Set by an overflow from timer A (table 7).

Timer A Interrupt Mask (IMTA: $001, Bit 3): Masks an interrupt request caused by the timer A interrupt request flag (table 8).

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): Set by an overflow from timer B (table 9).

Table 4 Interrupt Enable Flag

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

Table 5 External Interrupt Request Flags

IF0, IF1, IF2, IF3	Interrupt Request
0	Disabled
1	Enabled

Table 6 External Interrupt Masks

IM0, IM1, IM2, IM3	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 7 Timer A Interrupt Request Flag

IFTA	Interrupt Request
0	Disabled
1	Enabled

Table 8 Timer A Interrupt Mask

IMTA	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 9 Timer B Interrupt Request Flag

IFTB	Interrupt Request
0	Disabled
1	Enabled

Timer B Interrupt Mask (IMTB: $002, Bit 1): Masks an interrupt request caused by the timer B interrupt request flag (table 10).

Timer C Interrupt Request Flag (IFTC: $002, Bit 2): Set by an overflow from timer C (table 11).

Timer C Interrupt Mask (IMTC: $002, Bit 3): Masks an interrupt request caused by the timer C interrupt request flag (table 12).

Serial 1 Interrupt Request Flag (IFS1: $003, Bit 0): Set when the octal counter counts the eighth clock signal or when data transmission stops, resetting the octal counter (table 13).

Serial 1 Interrupt Mask (IMS1: $003, Bit 1): Masks an interrupt request caused by the serial 1 interrupt request flag (table 14).

Serial 2 Interrupt Request Flag (IFS2: $022, Bit 2): Set when the octal/hexadecimal counter counts the eighth/sixteenth clock signal or when data transmission stops, resetting the octal/hexadecimal counter (table 15).

Serial 2 Interrupt Mask (IMS2: $022, Bit 3): Masks an interrupt request caused by the serial 2 interrupt request flag (table 16).

Table 10 Timer B Interrupt Mask

IMTB	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 11 Timer C Interrupt Request Flag

IFTC	Interrupt Request
0	Disabled
1	Enabled

Table 12 Timer C Interrupt Mask

IMTC	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 13 Serial 1 Interrupt Request Flag

IFS1	Interrupt Request
0	Disabled
1	Enabled

Table 14 Serial 1 Interrupt Mask

IMS1	Interrupt Request
0	Enabled
1	Disabled (masked)

Table 15 Serial 2 Interrupt Request Flag

IFS2	Interrupt Request
0	Disabled
1	Enabled

Table 16 Serial 2 Interrupt Mask

IMS2	Interrupt Request
0	Enabled
1	Disabled (masked)

Key Scan Interrupt Request Flag (IFKS: $003, Bit 2): Set when the VFD controller enters key scan mode (table 17).

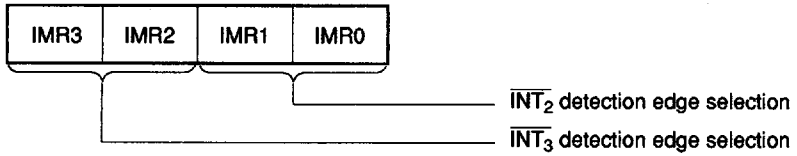
Key Scan Interrupt Mask (IMKS: $003, Bit 3): Masks an interrupt request caused by the key scan interrupt request flag (table 18).

Table 17 Key Scan Interrupt Request Flag

IFKS	Interrupt Request
0	Disabled
1	Enabled

Table 18 Key Scan Interrupt Mask

IMKS	Interrupt Request
0	Enabled
1	Disabled (masked)



IMR		
Bit 3	**Bit 2**	**$\overline{INT_3}$ Detection Edge**
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection

IMR		
Bit 1	**Bit 0**	**$\overline{INT_2}$ Detection Edge**
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection

Figure 13 Interrupt Mode Register

Operating Modes

The MCU has two internal oscillation circuits as shown in the block diagram of figure 22. The oscillation clocks are used in the state shown in figure 14.

Five operating modes are available, specified by how the clock is used, as shown in table 19. The functions available in each mode are listed in table 20, I/O states are listed in table 21, and transitions between operating modes are listed in figure 14.

Active Mode: The MCU operates according to the clock generated by the system oscillator.

Standby Mode: The MCU enters standby mode if the SBY instruction is executed from active mode. In this mode, the oscillator remains active, and the interrupts, the timer/counters, and the serial interface are enabled, but all instruction-control clocks stop. The stopping of these clocks stops the CPU, retaining all RAM and register contents and maintaining the current I/O pin status.

Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. In the latter case, the MCU becomes active and executes the next instruction following the SBY instruction. If the interrupt enable flag is 1 when an interrupt request is asserted, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. A flowchart of operation in standby mode is shown in figure 15.

Table 19 Low-Power Dissipation Modes

		System Clock (ϕ_{CPU})	
		Operating	**Stopped**
Non-time-base peripheral function clock (ϕ_{PER})	Operating	Active mode (LSON = 0)	Standby mode
	Stopped	Subactive mode (optional) (LSON = 1)	Watch mode (TMA3 = 1)
			Stop mode (TMA3 = 0)

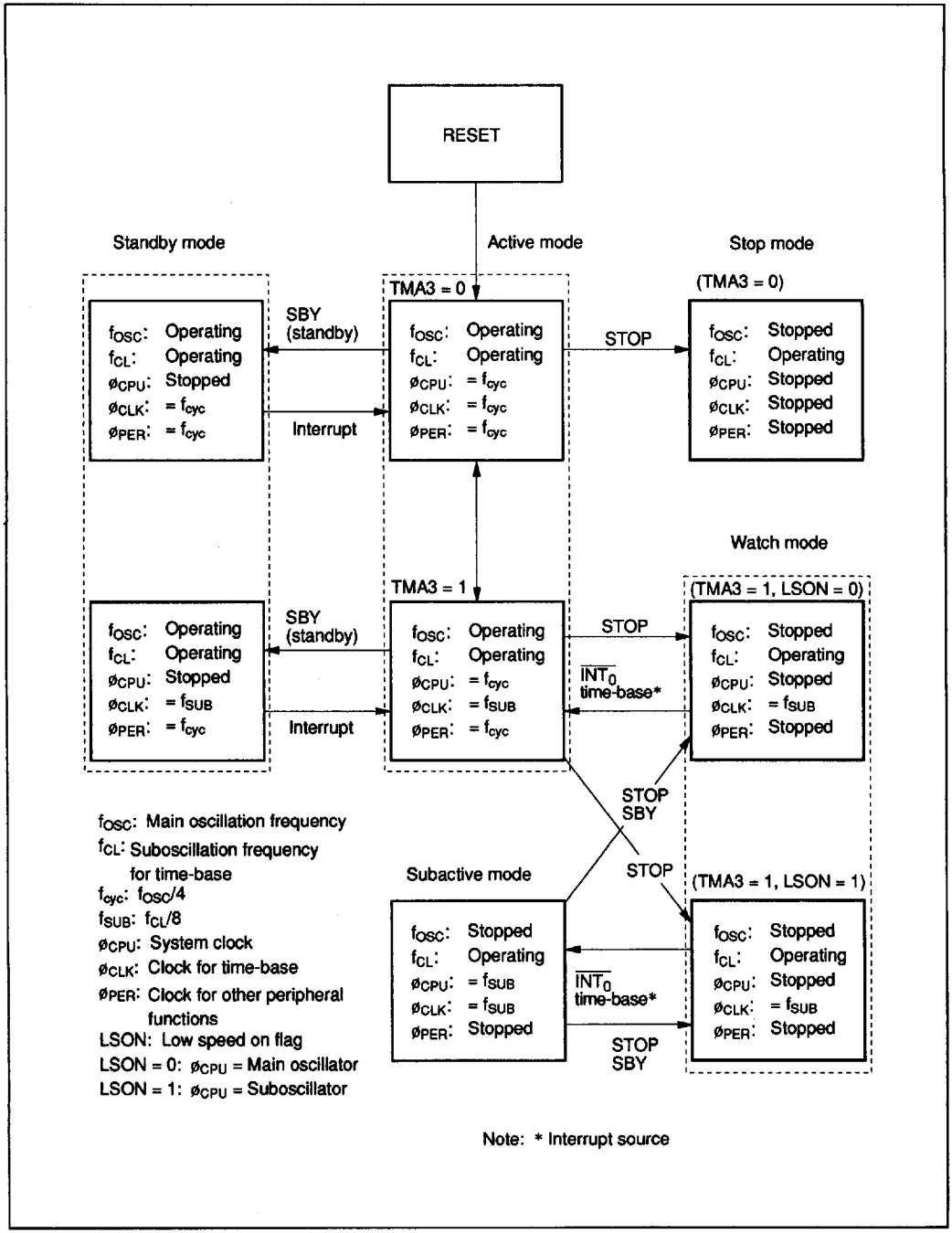


Figure 14 MCU Status Transitions

Table 20 Operations in Low-Power Dissipation Modes

Function		Stop Mode	Watch Mode	Standby Mode	Active Mode	Subactive Mode*6
System oscillator		Stopped	Stopped			Stopped
Subsystem oscillator		*1				
CPU operation (ϕ_{CPU})	Instruction execution	Stopped	Stopped	Stopped		
	RAM	Retained	Retained	Retained		
	Registers, flags	Reset	Retained	Retained		
	I/O*2	Reset	Retained	Retained		
Peripheral functions, interrupts (ϕ_{PER})	$\overline{INT_0}$	Reset	Retained			Retained
	$\overline{INT_1}$–$\overline{INT_3}$	Reset	Retained			Retained
	Timer A	Reset	Retained			Retained
	Timer B	Reset	Retained			Retained
	Timer C	Reset	Retained			Retained
	Serial 1, Serial 2	Reset	Retained			Retained
	VFD	Reset	Retained/ Reset*3	*7		Retained/ Reset*3
	PWM	Reset	Retained/ Reset*3			Retained/ Reset*3
Time-base functions, interrupts (ϕ_{CLK})	$\overline{INT_0}$	Reset	*4	*5	*5	*4
	Time-base	Reset	*4	*5	*5	*4

Notes: ■ indicates operating.

1. To reduce I_{CC}, stop all oscillation in external circuits.
2. Refer to table 21.
3. Only the timing generator is reset. The contents of the mode registers are retained.
4. Refer to the Interrupt Frame section.
5. If TMA3 is set to 1, timer A and $\overline{INT_0}$ are switched to time-base function and interrupt, respectively.
6. Subactive mode is an optional function.
7. VFD is active, but it displays nothing because the display data RAM is not working.

Table 21 Input/Output in Low-Power Dissipation Modes

	Output		Input
	Standby Mode	Stop/Watch/ Subactive Mode	All Modes (Input state)
D_0–D_{15}	Retained/peripheral function output	High impedance	Input enabled
R0–RA	Retained/peripheral function output	High impedance	Input enabled

Note: Applying a voltage between (V_{CC} – 0.3) and (GND + 0.3 V) to input-state pins increases the current between V_{CC} and GND.

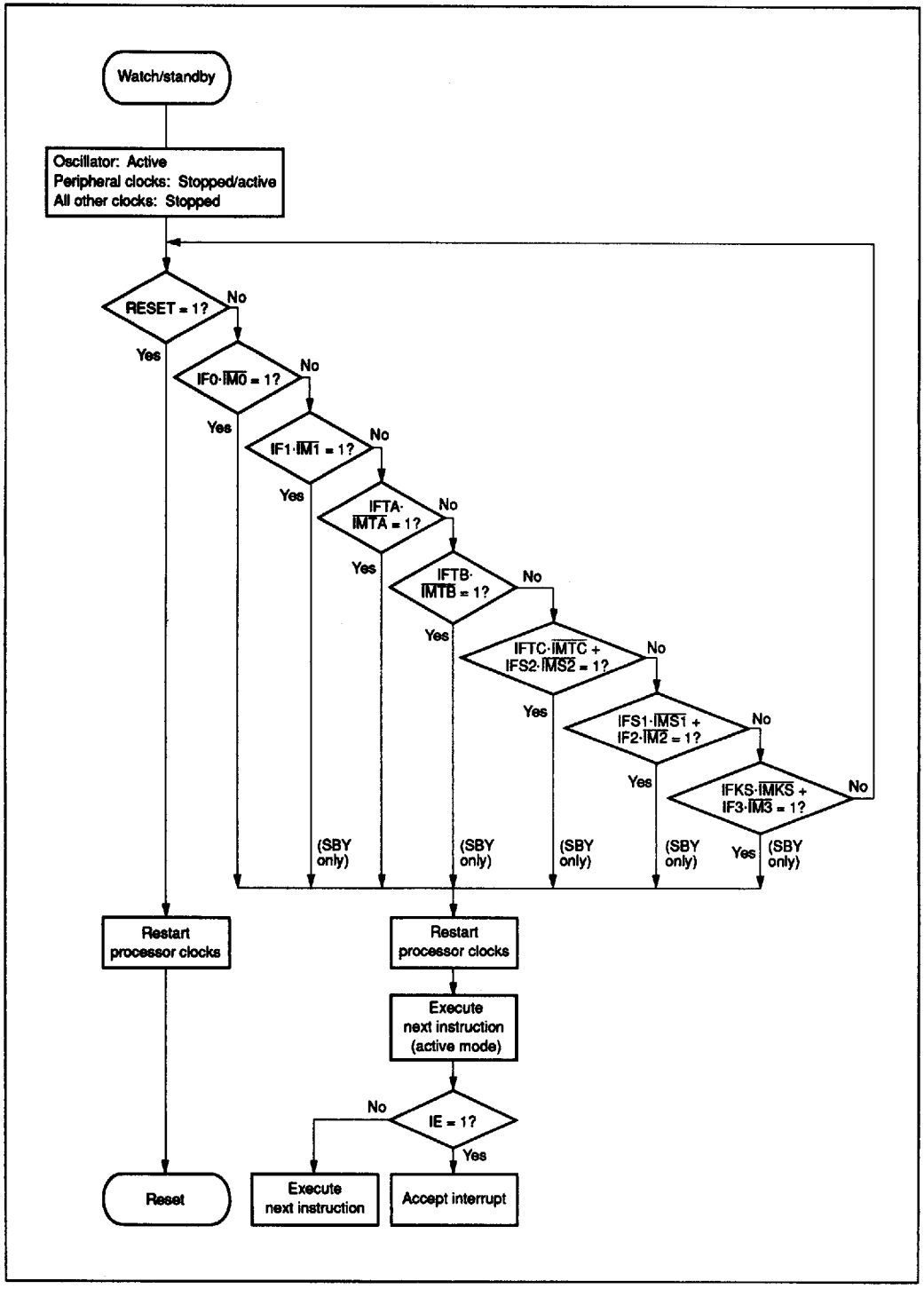


Figure 15 Flowchart of Watch and Standby Modes

Stop Mode: The MCU enters stop mode if the STOP instruction is executed in active mode while TMA3 = 0. In this mode, the system oscillator stops, causing all MCU functions to stop as well.

The stop mode is terminated by a RESET input as shown in figure 16. RESET must be high for at least one t_{RC} to stabilize oscillation (refer to the AC Characteristics table). In stop mode, all RAM contents are retained.

After stop mode is cancelled, the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register cannot be guaranteed.

Watch Mode: The MCU enters watch mode if the STOP instruction is executed in active mode while TMA3 = 1, or if the STOP/SBY instruction is executed in subactive mode.

The watch mode is terminated by a RESET input or a timer-A/$\overline{INT_0}$ interrupt request. For details of RESET input, refer to the Stop Mode section. When terminated by a timer-A/$\overline{INT_0}$ interrupt request, the MCU enters active mode if LSON is 0 or subactive mode if LSON is 1. Any interrupt request generated for the transition to active mode is delayed for half the interrupt frame period (t_{RC}) to give the oscillation time to stabilize (figure 17). Operation during mode transition is the same as that at standby mode cancellation (figure 15).

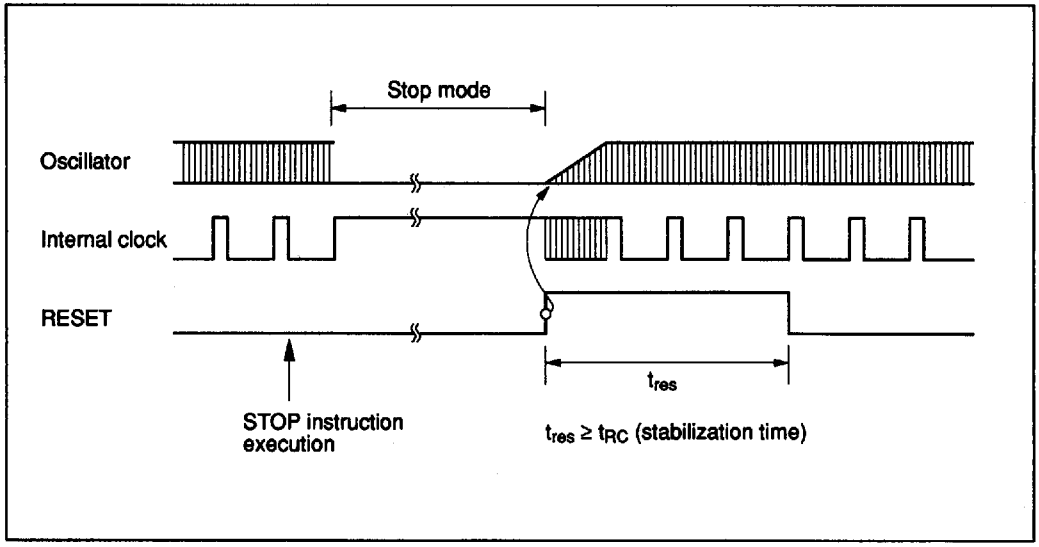


Figure 16 Timing of Stop Mode Cancellation

Subactive Mode: The CPU operates with a clock generated by the CL_1 and CL_2 oscillation circuits. Functions which can operate in subactive mode are listed in table 20.

The subactive mode is an optional function that the user must specify on the function option list.

Interrupt Frame: In watch and subactive modes, ϕ_{CLK} is supplied for timer A and the $\overline{INT_0}$ circuit. Prescaler W and timer A operate as time bases to generate interrupt frame timing. Three interrupt frame cycles (T) can be selected by the settings of miscellaneous register 1, as shown in figures 17 and 18.

In watch and subactive modes, timer A and $\overline{INT_0}$ interrupts are generated in synchronism with the interrupt frame. An interrupt request is generated at the interrupt strobe timing, except when the MCU enters active mode from watch mode. The $\overline{INT_0}$ falling edge is acknowledged regardless of the interrupt frame, but the interrupt is executed simultaneously with the next interrupt strobe. Timer A generates an overflow and interrupt request at the timing of an interrupt strobe.

MCU Operation Sequence: The MCU operates in the sequence shown in figures 19 to 21. It is reset by an asynchronous RESET input, regardless of its state.

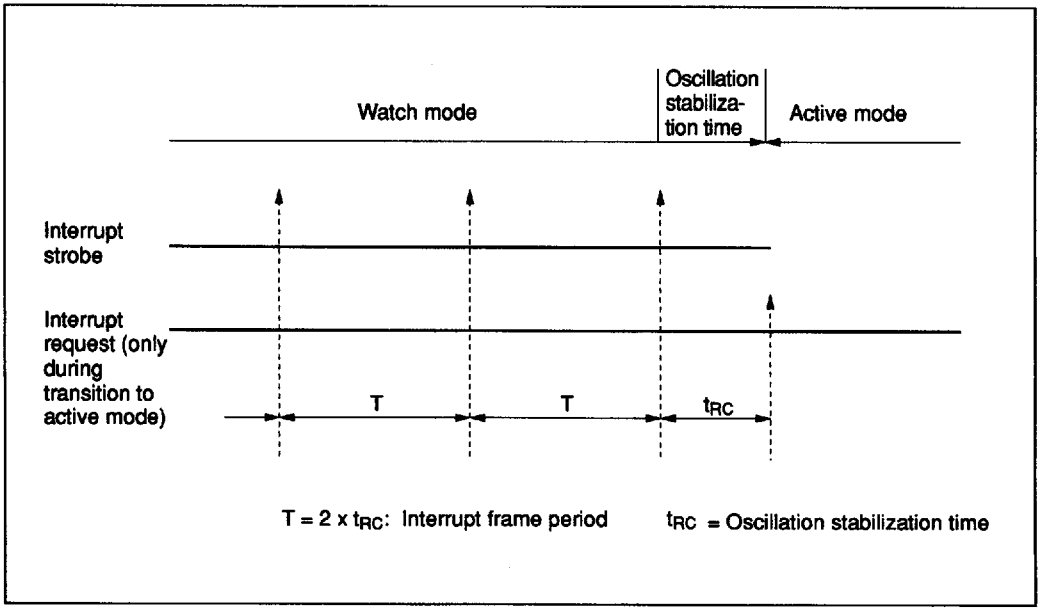
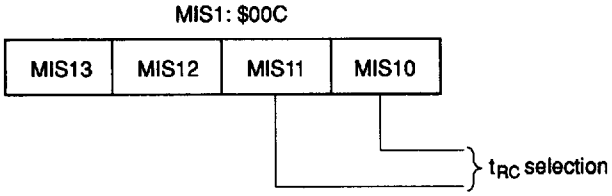


Figure 17 Interrupt Frame



MIS1

Bit 1	Bit 0	T/2, t_{RC}
0	0	0.12207 ms
0	1	7.8125 ms
1	0	62.5 ms
1	1	Not used

Note: For 32.768-kHz oscillation only
T: Interrupt frame length
t_{RC}: Oscillation stabilization time

Figure 18 Miscellaneous Register 1

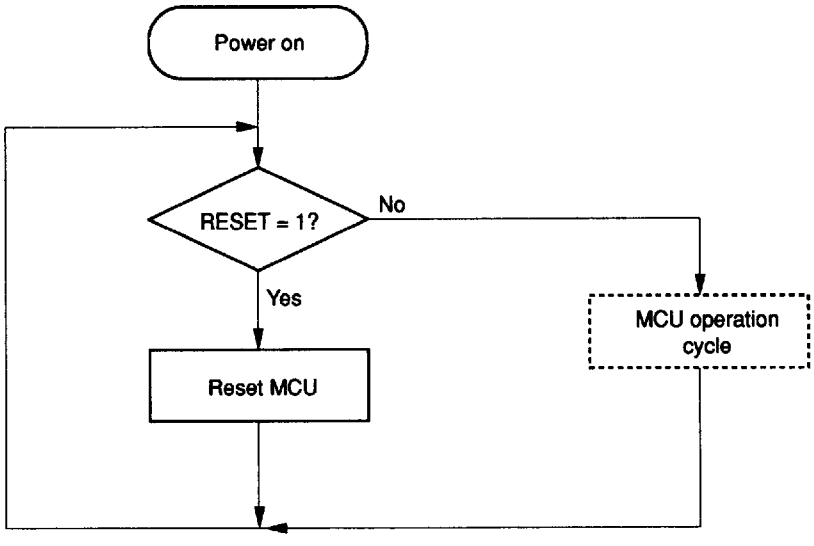
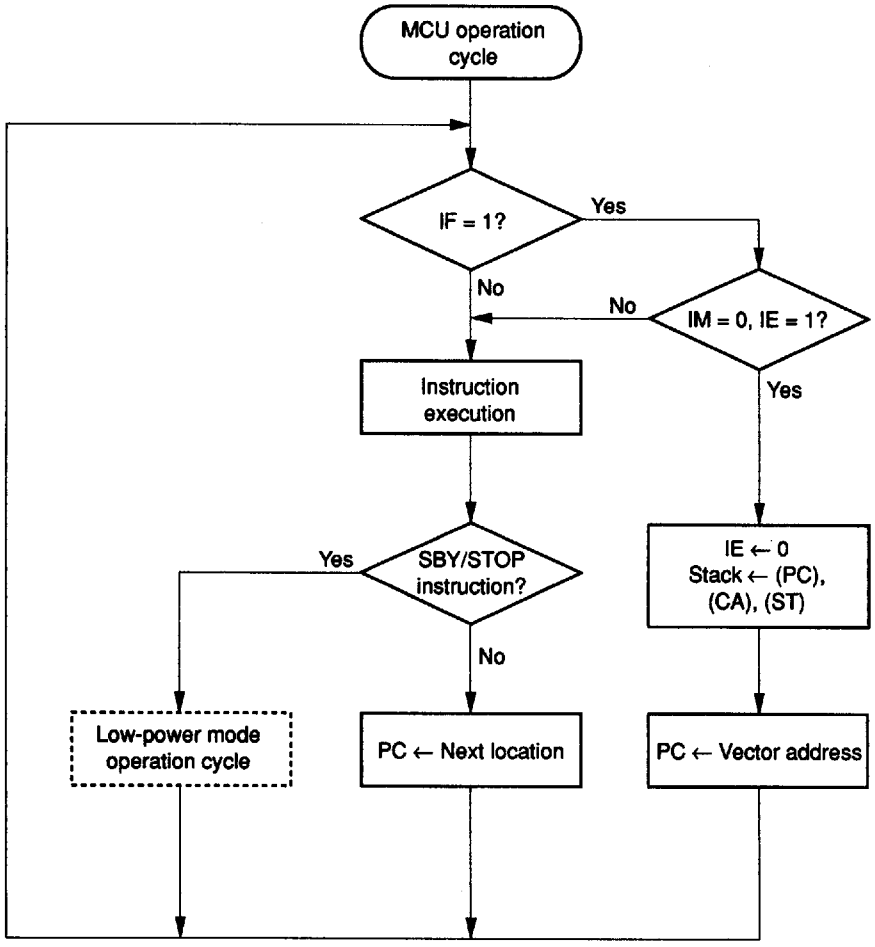


Figure 19 MCU Operation Flowchart (Power On)



IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
PC: Program counter
CA: Carry flag
ST: Status flag

Figure 20 MCU Operation Flowchart (MCU Operation Cycle)

The low-power mode operation sequence is shown in figure 21. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

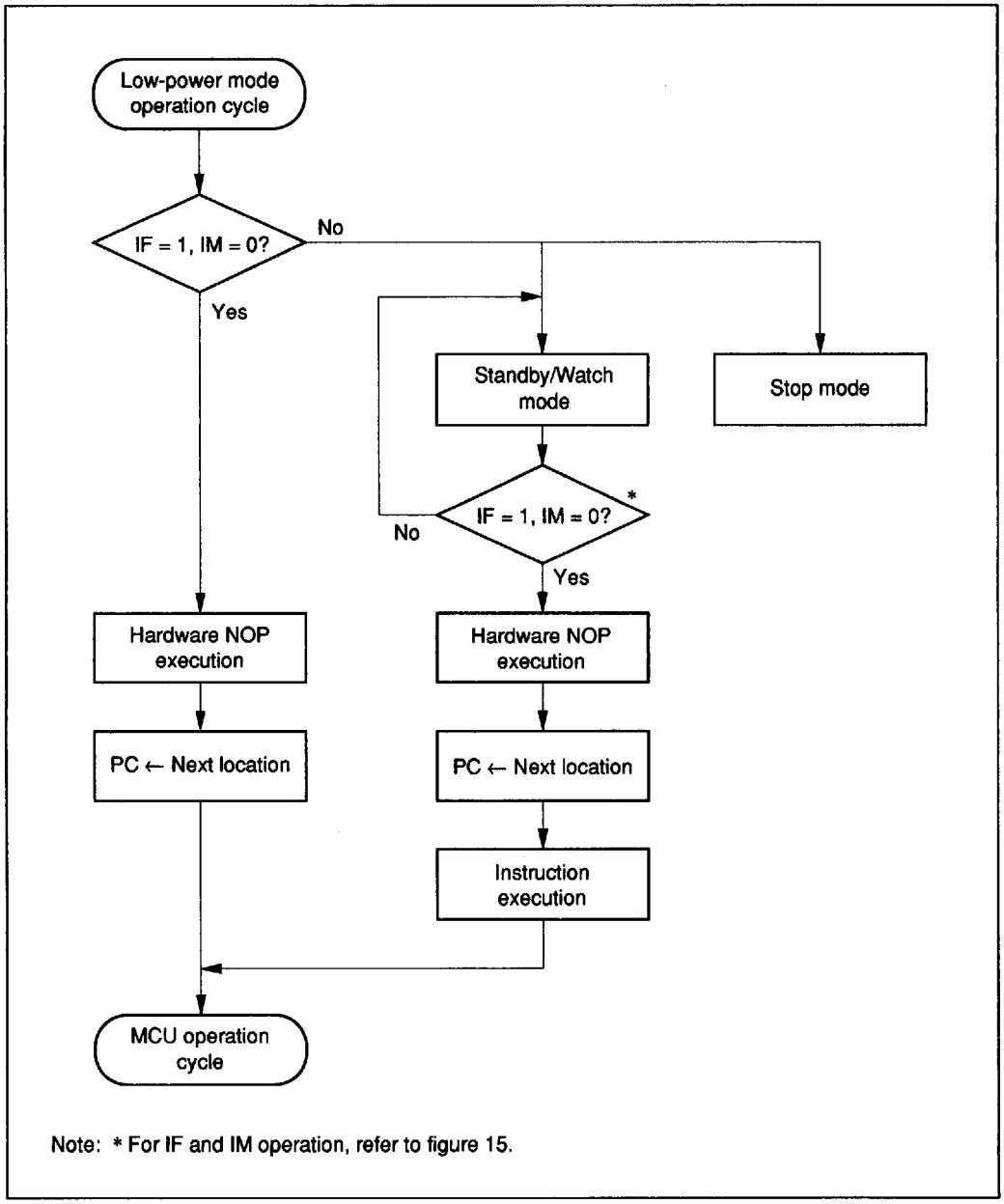


Figure 21 MCU Operation Flowchart (Low-Power Dissipation Mode Operation)

Internal Oscillation Circuit

A block diagram of the internal oscillation circuit is shown in figure 22. As shown in table 22, a crystal or ceramic oscillator can be connected to OSC_1 and OSC_2, and a crystal oscillator of 32.768 kHz can be connected to CL_1 and CL_2. An external clock operation of the system oscillator is also available.

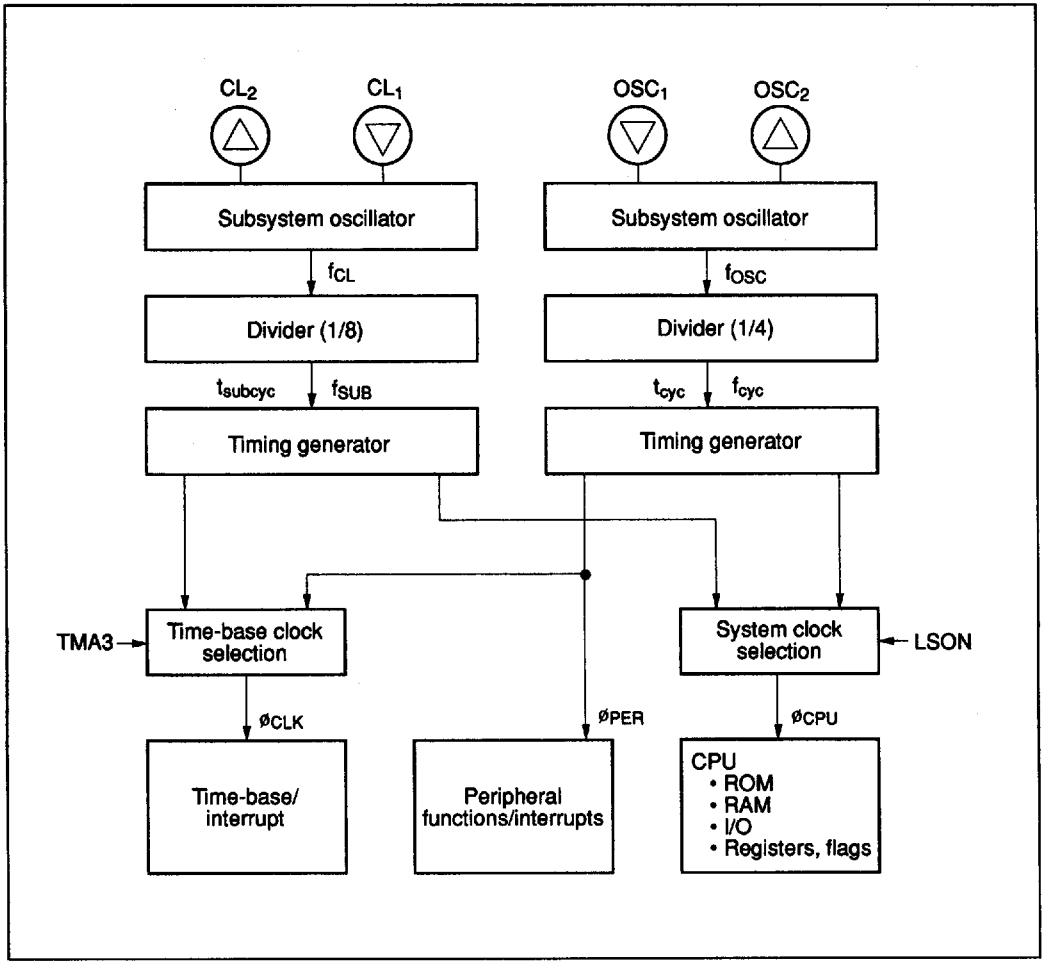


Figure 22 Internal Oscillator Circuit

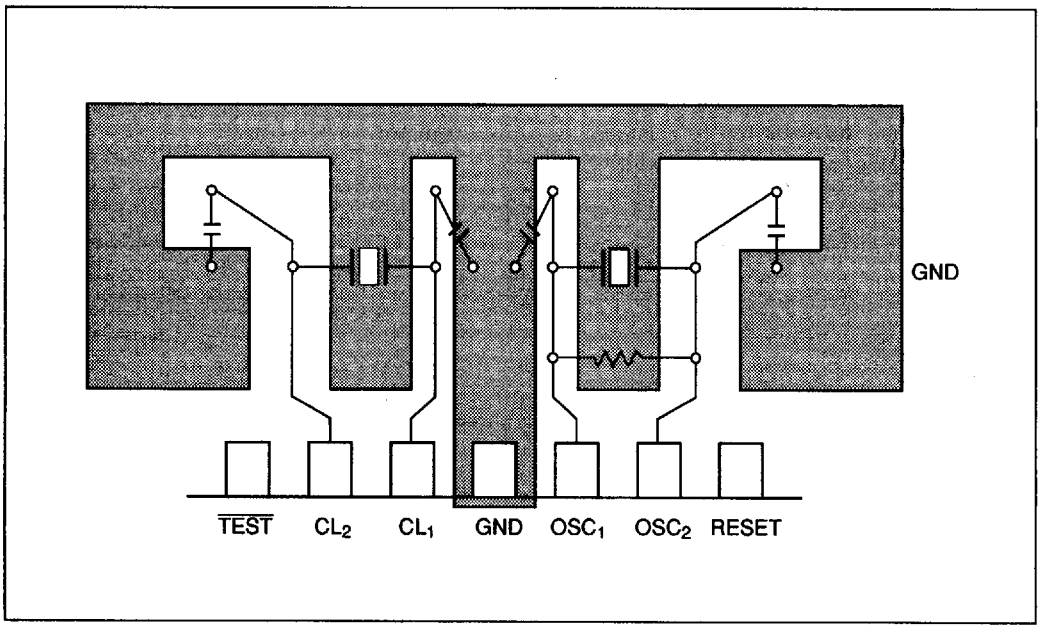
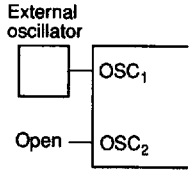
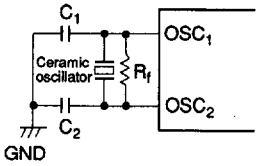
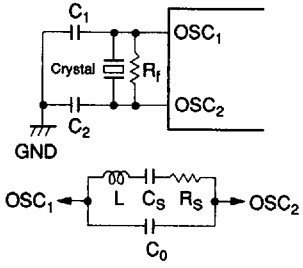
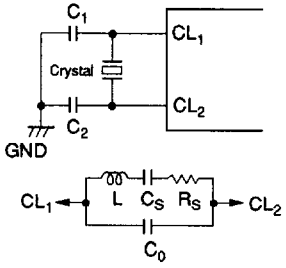


Figure 23 Typical Layout of Crystal or Ceramic Oscillator

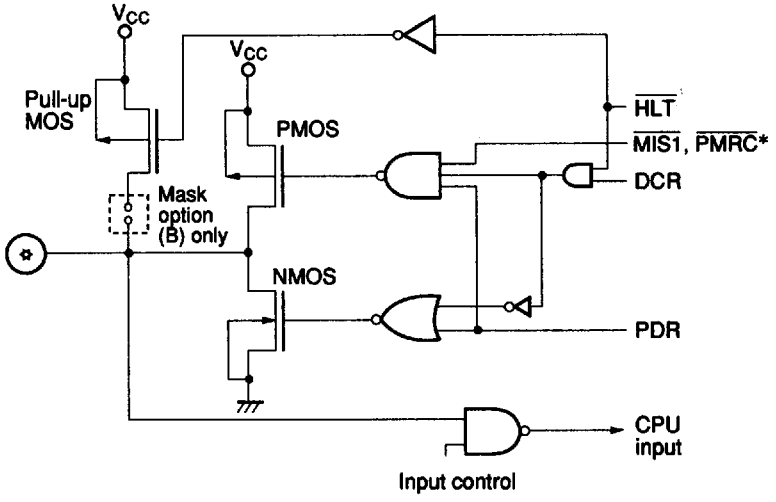
Table 22 Oscillator Circuit Examples

Circuit Configuration		Circuit Constants
External clock operation (OSC_1, OSC_2)		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator: CSA4.00MG (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 30 pF ± 20%
Crystal oscillator (OSC_1, OSC_2)		R_f = 1 MΩ ± 20% $C_1 = C_2$ = 10 pF ± 20% Crystal: Equivalent to circuit shown at bottom left C_0 = 7 pF, max. R_S = 100 Ω, max. f = 1.6 to 4.5 MHz
Crystal oscillator (CL_1, CL_2)		$C_1 = C_2$ = 15 pF ± 5% Crystal: Equivalent to circuit shown at bottom left MX38T (Nihon Denpa Kogyo) C_0 = 1.5 pF, typ. R_S = 14 kΩ, typ. f = 32.768 kHz

Notes:
1. The circuit constants given above are recommended values provided by the oscillator manufacturer. Since they may be affected by stray capacitances from the oscillator or board, consult the crystal or ceramic oscillator manufacturer to determine the actual circuit parameters required.
2. Wiring between the OSC_1/OSC_2 pins (CL_1/CL_2 pins) and other elements must be as short as possible, and must not cross other wiring. Refer to the recommended layout of the crystal and ceramic oscillator in figure 23.
3. If not using a 32.768-kHz crystal oscillator, fix the CL_1 pin to GND and leave the CL_2 pin open.

Input/Output

The MCU has 50 input/output pins and 6 input pins, 32 of the input/output pins being high-voltage, high-current pins which are multiplexed with the VFD controller pins. The standard pin output buffer is turned on and off by the combination values in the port data register (PDR) and data control register (DCR), as shown in figure 24.



Mask Option		With Pull-up MOS (B)				Without Pull-up MOS (C)			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-up MOS		On	On	On	On	—	—	—	—

Notes: —: Off

* For the $R4_2/SO_1$ pin, the PMOS is off when bit 2 of miscellaneous register 1 (MIS12) is set to 1. For the $R7_3/SO_2$ pin, the PMOS is off when bit 3 of port mode register C (PMRC) is set to 1.

MIS1 Bit 2	$R4_2/SO_1$ Output Mode
0	CMOS
1	NMOS open drain

PMRC Bit 3	$R7_3/SO_2$ Output Mode
0	CMOS
1	NMOS open drain

Figure 24 Input/Output Buffer

D Port: Comprised of 16 of the 50 I/O pins, they are discrete pins (D port) that are accessed individually. These pins are set by the SED and SEDD instructions, reset by the RED and REDD instructions, and tested by the TD and TDD instructions. Pins D_0 to D_{15} are multiplexed with VFD controller pins FS_{15} to FS_0, respectively. Circuits of the D port are shown in table 23.

R Ports: Accessed in 4-bit units. Data is input to the ports by the LAR and LBR instructions and output from them by the LRA and LRB instructions. The R4 to R8 output buffers are turned on and off by R-port data control registers (DCR4–DCR8). Pins $R4_0$–$R4_3$, $R6_0$–$R6_3$, and $R7_0$–$R7_3$ are multiplexed with pins $\overline{SCK_1}$, SI_1, SO_1, PWM, $\overline{INT_0}$–$\overline{INT_3}$, BUZZ, $\overline{SCK_2}$, SI_2, and SO_2, respectively. Circuits of the R ports are shown in table 23, and pin mode selection registers are shown in figure 25.

Mask Options: The circuits of the HD4074729 and HD4074720 are either without pull-up MOS (C) or without pull-down MOS (D), as shown in table 23. Options either with pull-up MOS (B) or with pull-down MOS (E) can be selected for the HD404728, HD404729 and HD404720 but note that these MCUs are not compatible with the HD4074729 and HD4074720. If with pull-down MOS (E) option is selected, the RA_1/V_{disp} pin must be set to the V_{disp} pin by the mask option because the source of the pull-down MOS is connected to V_{disp}.

How to Deal with Unused I/O Pins: I/O pins that are not needed by the user system must be connected to V_{CC} to prevent LSI malfunctions due to noise. Note the following precautions:

The without pull-down MOS option must be selected for high-voltage pins and the without pull-up MOS option must be selected for standard pins. The contents of the PDR and DCR of a pin selected by program must be retained in the same way as for a reset. Do not select such pins to be peripheral function I/O pins.

Table 23 Input/Output Pin Types

Standard Pins

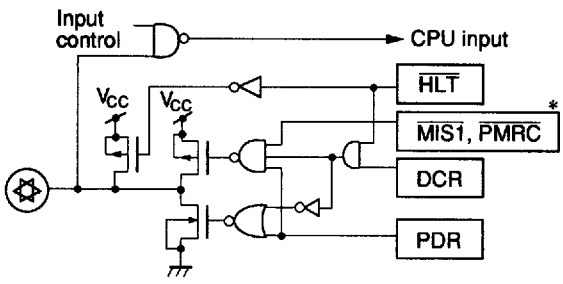
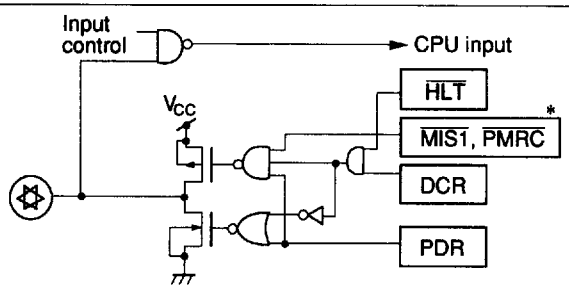
Pin Type	With Pull-Up MOS (B)/Without Pull-Up MOS (C)	Pin Name
I/O pins	 Note: * Applies to $R4_2$ and $R7_3$.	$R4_0$–$R4_3$ $R5_0$–$R5_3$ $R6_0$–$R6_3$ $R7_0$–$R7_3$ $R8_0$–$R8_1$
	 Note: * Applies to $R4_2$ and $R7_3$.	

Table 23 Input/Output Pin Types (cont)

Standard Pins

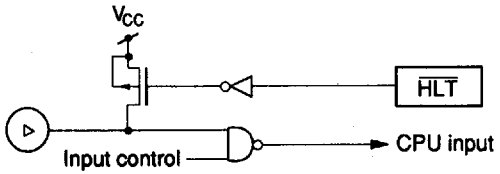
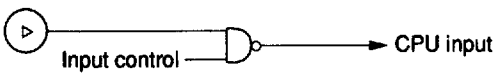
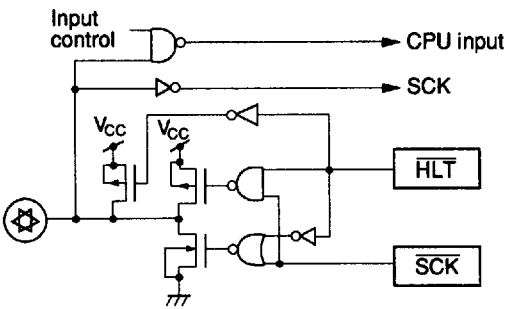
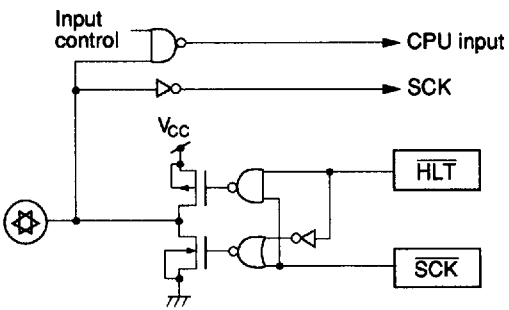
Pin Type	With Pull-Up MOS (B)/Without Pull-Up MOS (C)	Pin Name
Input pins		$R9_0$–$R9_3$
		
Peripheral I/O pins		$\overline{SCK_1}$ $\overline{SCK_2}$ (output)*1
		

Table 23 Input/Output Pin Types (cont)

Standard Pins

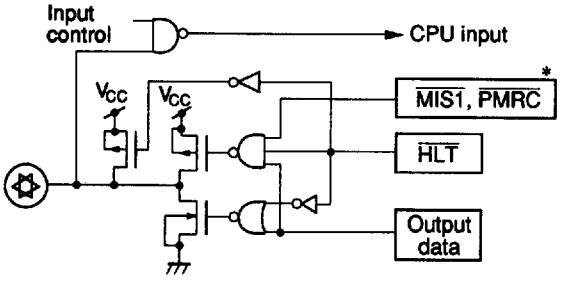
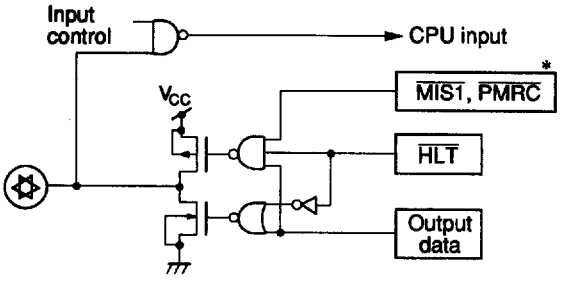
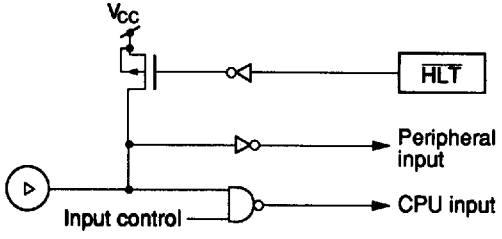
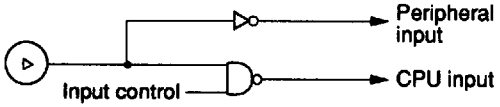
Pin Type	With Pull-Up MOS (B)/Without Pull-Up MOS (C)	Pin Name
Peripheral output pins	 Note: * Applies to SO_1 and SO_2.	SO_1, SO_2 PWM BUZZ
	 Note: * Applies to SO_1 and SO_2.	
Peripheral input pins		$\overline{SCK}_1$, $\overline{SCK}_2$ (input)*1 SI_1, SI_2 $\overline{INT}_0$ $\overline{INT}_1$ $\overline{INT}_2$ $\overline{INT}_3$
		

Table 23 Input/Output Pin Types (cont)

High-Voltage Pins

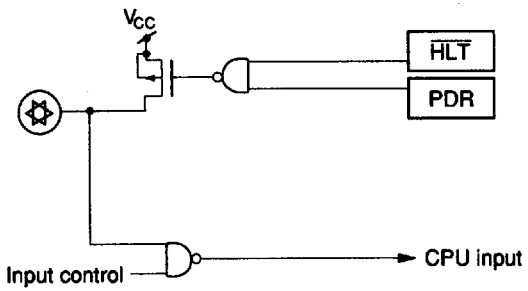
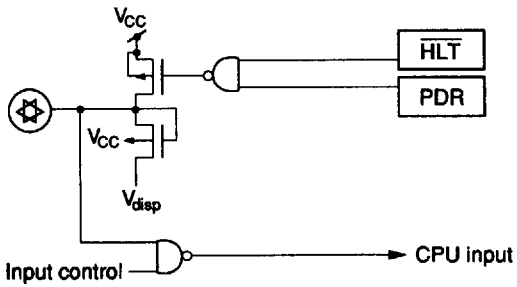
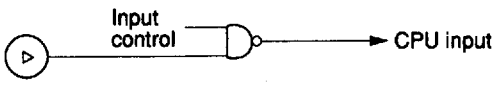
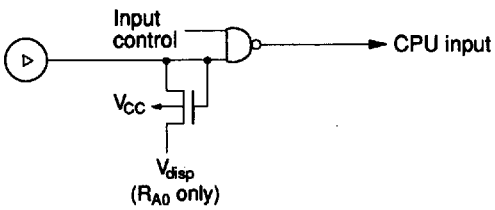
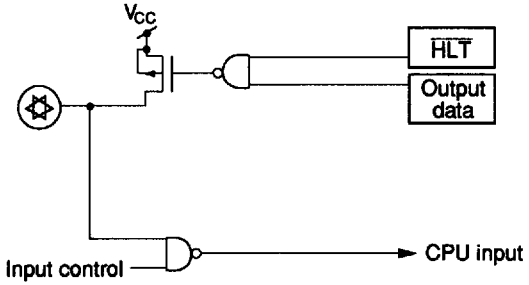
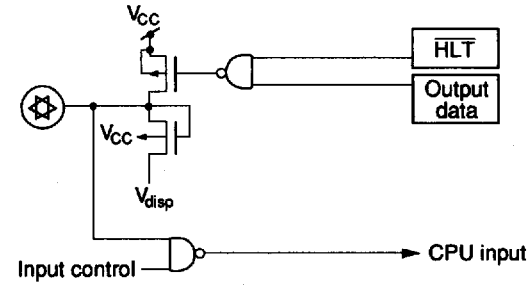
Pin Type	Without Pull-Down MOS (D)/With Pull-Down MOS (E)	Pin Name
I/O pins		D_0–D_{15} $R0_0$–$R0_3$ $R1_0$–$R1_3$ $R2_0$–$R2_3$ $R3_0$–$R3_3$
		
Input pins		RA_0–RA_1
		

Table 23 Input/Output Pin Types (cont)

High-Voltage Pins

Pin Type	Without Pull-Down MOS (D)/With Pull-Down MOS (E)	Pin Name
Peripheral output pins		FS_0–FS_{15} FD_0–FD_{15}
		

Notes:
1. If external clock mode is selected when the serial interface is used, $\overline{SCK_1}$ and $\overline{SCK_2}$ are used as input pins.
2. In stop mode, the MCU is internally reset and peripheral functions are cancelled. The HLT signal goes high and the output pins are at high impedance.
3. In watch/subactive mode, the HLT signal goes high and the output pins are at high impedance. The input level of I/O pins selected for peripheral functions must be fixed since these pins are in input state.
4. Select the circuit type for a mask ROM MCU as shown below. A mask ROM MCU is compatible with a ZTAT™ MCU only when C- and D-type circuits are selected for the mask ROM MCU.

	Circuit Type			
Product Type	**B**	**C**	**D**	**E**
Mask ROM (HD404728, HD404729, HD404720)		Optional		
ZTAT™ (HD4074729, HD4074720)		Fixed		

MIS1 (miscellaneous register 1) ADR: $00C

MIS13	MIS12	MIS11	MIS10

$R4_2/SO_1$ pin PMOS mode selection
$R7_0$/BUZZ pin mode selection

MIS1 Bit 3	Port Selection
0	$R7_0$
1	BUZZ

SMRA (serial mode register A) ADR: $005

SMRA3	SMRA2	SMRA1	SMRA0

$R4_0/\overline{SCK_1}$ pin mode selection

SMRB (serial mode register B) ADR: $01B

SMRB3	SMRB2	SMRB1	SMRB0

$R7_0/\overline{SCK_2}$ pin mode selection

SMRA Bit 3	Port Selection
0	$R4_0$
1	$\overline{SCK_1}$

SMRB Bit 3	Port Selection
0	$R7_1$
1	$\overline{SCK_2}$

PMRA (port mode register A) ADR: $004

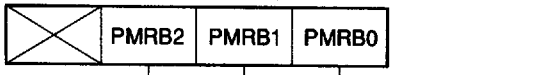
PMRA3	PMRA2	PMRA1	PMRA0

$R4_2/SO_1$ pin mode selection
$R4_1/SI_1$ pin mode selection
$R6_0/\overline{INT_0}$ pin mode selection
$R6_1/\overline{INT_1}$ pin mode selection

PMRA Bit 3	Port Selection	PMRA Bit 2	Port Selection	PMRA Bit 1	Port Selection	PMRA Bit 0	Port Selection
0	$R6_1$	0	$R6_0$	0	$R4_1$	0	$R4_2$
1	$\overline{INT_1}$	1	$\overline{INT_0}$	1	SI_1	1	SO_1

Figure 25 Pin Mode Selection Registers

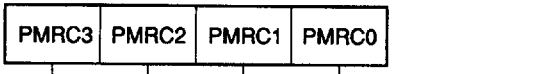
PMRB (port mode register B) ADR: $015



$R6_2/\overline{INT_2}$ pin mode selection
$R6_3/\overline{INT_3}$ pin mode selection
$R4_3$/PWM pin mode selection

PMRB Bit 2	Port Selection	PMRB Bit 1	Port Selection	PMRB Bit 1	Port Selection
0	$R4_3$	0	$R6_3$	0	$R6_2$
1	PWM	1	$\overline{INT_3}$	1	$\overline{INT_2}$

PMRC (port mode register C) ADR: $01A



$R7_3/SO_2$ pin mode selection
$R7_2/SI_2$ pin mode selection
8/16 serial 2-bit length selection
$R7_3/SO_2$ pin PMOS mode selection

PMRC Bit 1	Port Selection	PMRC Bit 0	Port Selection
0	$R7_2$	0	$R7_3$
1	SI_2	1	SO_2

Figure 25 Pin Mode Selection Registers (cont)

Timers

The MCU has two prescalers (S and W) and three timer/counters (A, B, and C). Block diagrams of the timers are shown in figures 26 and 27. The functions of the three timers are selected by software as shown in table 24.

Prescaler S: Eleven-bit counter that inputs a system clock signal. After being initialized to $000 by MCU reset, prescaler S divides the system clock frequency. In watch and subactive modes, prescaler S stops counting and retains its value. When these modes are cancelled, it resumes counting. Of the prescaler S outputs, timer A input clock, timer B input clock, timer C input clock, and serial interface transmit clock are selected by timer mode register A (TMA), timer mode register B (TMB), timer mode register C (TMC), and serial mode registers A and B (SMRA, SMRB), respectively.

Prescaler W: Five-bit counter that inputs the CL_1 input clock signal divided by 8. After being initialized to $00 by MCU reset, prescaler W divides the input clock. Prescaler W output can be selected as a timer A input clock by timer mode register A. In this case, prescaler W and timer A can be reset by software.

Table 24 Timers A, B, and C Functions Selection

Timer A Condition	Function
TMA3 = 0	System clock base interval timer
TMA3 = 1	Time-base for clock

Timer B Condition	Function
TMB2–TMB0 ≠ 111	Automatic reloading timer
TMB2–TMB0 = 111 and PMRA3 = 1	Event counter (using $R6_1/\overline{INT_1}$)

Timer C Condition	Function
WDON = 0 (MIS13 = 1)	Automatic reloading timer (square-wave output circuit using $R7_0$/BUZZ)
WDON = 1	Watchdog timer

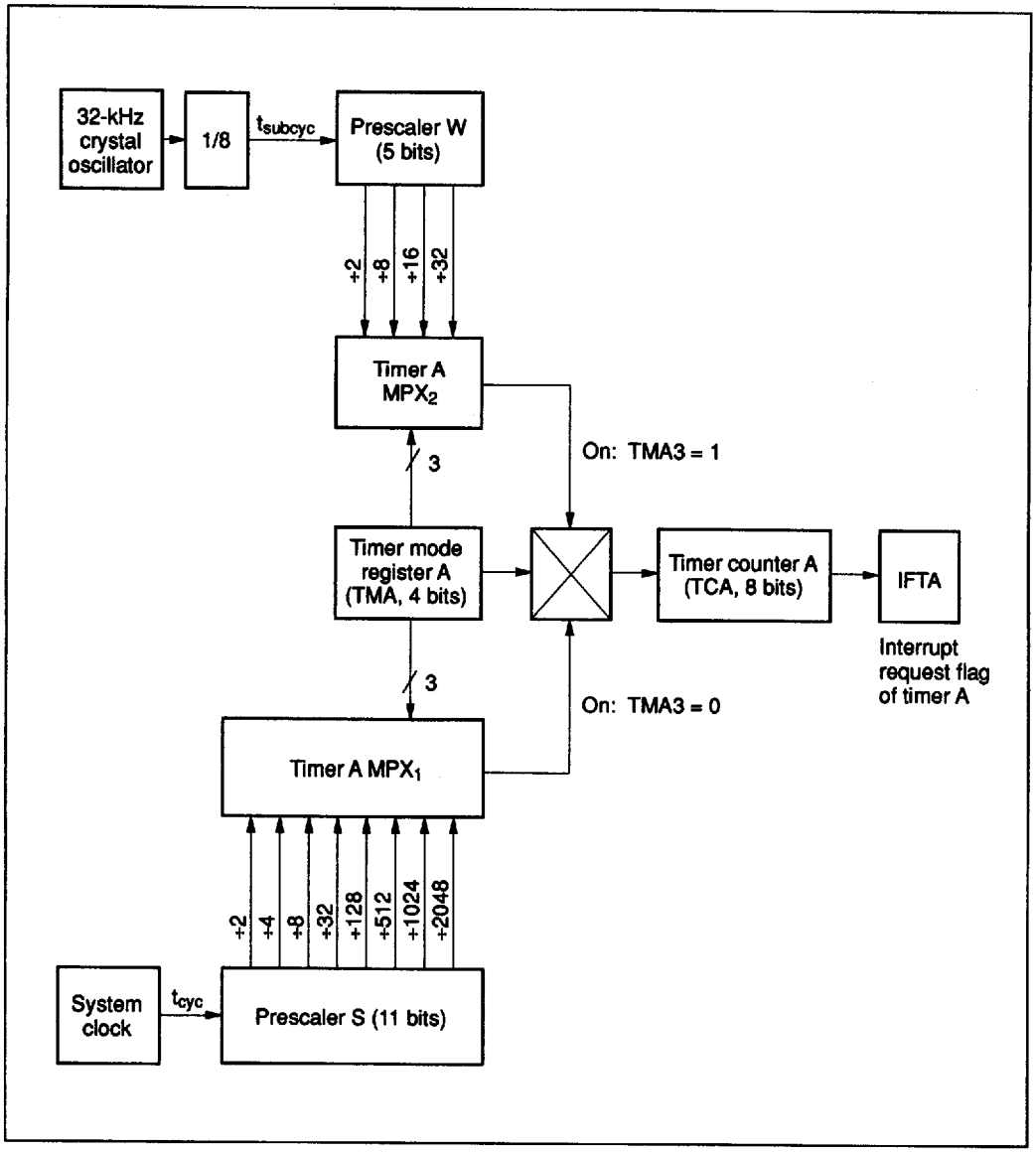


Figure 26 Block Diagram of Timer A

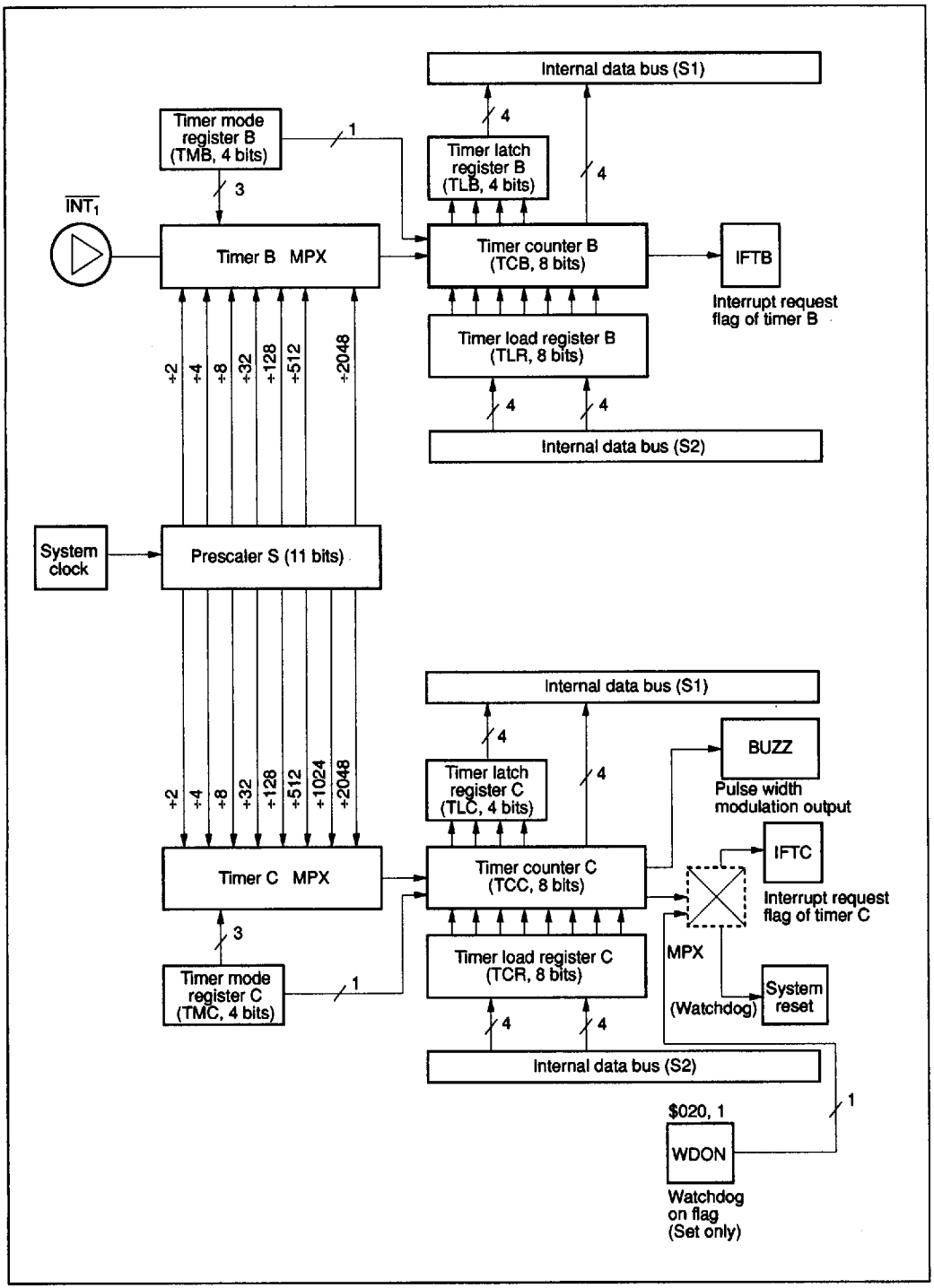


Figure 27 Block Diagram of Timer B and C

Timer A: Eight-bit timer which can be used as a clock time base. Timer A is initialized to $00 by reset, then incremented by each input clock. If an input clock is applied to timer A after it has reached $FF, an overflow that sets the timer A interrupt request flag (IFTA: $001, bit 2) is generated, and timer A restarts from $00. Timer A is an interval timer which overflows every 256 clock inputs.

Timer A can also be used as a clock time base when the TMA3 bit of timer mode register A (TMA) is set to 1. The timer is driven by the 32.768-kHz oscillator clock frequency divided by prescaler W. In this case, prescaler W and timer A can be initialized by software. The input clock of timer A is controlled by TMA.

Timer B (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Eight-bit write-only timer load register (TLRL and TLRU) and read-only timer counter (TCBL and TCBU) located at the same address. The eight-bit configuration consists of lower and upper digits located at sequential addresses.

Timer counter B is initialized by writing data to timer load register B (TLR). In this case, the lower digit must be written first. Both the upper and lower digits of TLR are loaded into the timer counter at the same time the upper digit is written to TLR. TLR is initialized to $00 by MCU reset.

The count of timer B is obtained by reading timer counter B. In this case, the upper digit must be read first; the count is latched at the same time the upper digit is read.

An automatic reloading function, input clock source, and prescaler division ratio of timer B are selected by timer mode register B (TMB). When an external event input is used as the input clock source of timer B, the $R6_1/\overline{INT_1}$ pin must be specified as the $\overline{INT_1}$ pin by port mode register A (PMRA: $004) and interrupt requests must be masked by the external interrupt mask bit (IM1).

Timer B is initialized to the value set in timer load register B (TLR) by software, and is then incremented by one every clock input. If an input clock is applied to timer B after it has reached $FF, an overflow is generated. In this case, if the automatic reloading function is enabled, timer B is initialized to its initial value; if reloading is disabled, the timer is initialized to $00. The overflow sets the timer B interrupt request flag (IFTB: $002, bit 0).

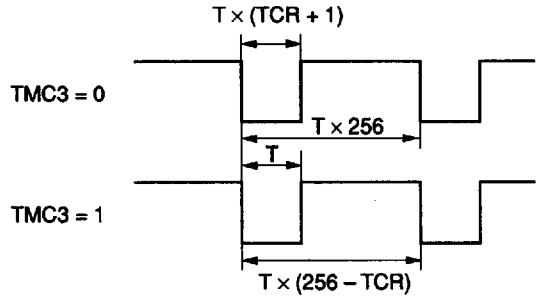
Timer C (TCCL: $00E, TCCU: $00F, TCRL: $00E, TCRU: $00F): Eight-bit write-only timer load register (TCRL and TCRU) and read-only timer counter (TCCL and TCCU) located at the same address. The eight-bit configuration consists of lower and upper digits located at sequential addresses. The operation of timer C is basically the same as that of timer B.

An automatic reloading function and prescaler division ratio of timer C depend on the state of timer mode register C (TMC). Timer C is initialized to the value set in the TMC by software, and is then incremented by one every clock input. If an input clock is applied to timer C after it has reached $FF, an overflow is generated. In this case, if the automatic reloading function is enabled, timer C is initialized to its initial value; if the function is disabled, the timer is initialized to $00. The overflow sets the timer C interrupt request flag (IFTC: $002, bit 2).

Timer C also functions as a watchdog timer. If a program routine goes out of control and an overflow is generated while the watchdog on flag (WDON) is set, the MCU is reset.

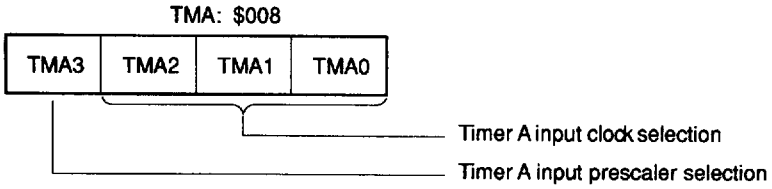
Timer C has a variable-duty pulse output (BUZZ) whose output waveform depends on the states of timer mode register C (TMC) and timer load register C (TCR) as shown in figure 28. For pulse output, the $R7_0$/BUZZ pin must be specified as BUZZ by miscellaneous register 1.

Timer Mode Register A (TMA: $008): Four-bit write-only register which controls timer A as shown in figure 29. It is initialized to $0 by MCU reset.



T: Period of clock input to the counter (figure 31)
TCR: Value of timer load register C (0–255)

Figure 28 Variable-Duty Pulse Output Waveform



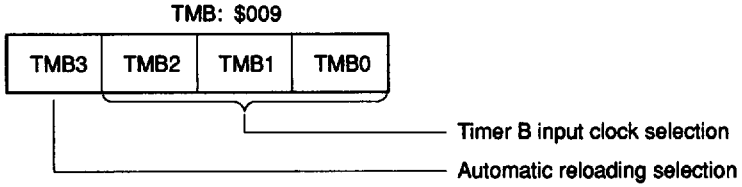
TMA3	TMA2	TMA1	TMA0	Source Prescaler, Input Clock Period, Operating Mode	
0	0	0	0	PSS, 2048 t_{cyc}	Timer A mode
			1	PSS, 1024 t_{cyc}	
		1	0	PSS, 512 t_{cyc}	
			1	PSS, 128 t_{cyc}	
	1	0	0	PSS, 32 t_{cyc}	
			1	PSS, 8 t_{cyc}	
		1	0	PSS, 4 t_{cyc}	
			1	PSS, 2 t_{cyc}	
1	0	0	0	PSW, 32 t_{subcyc}	Time-base mode
			1	PSW, 16 t_{subcyc}	
		1	0	PSW, 8 t_{subcyc}	
			1	PSW, 2 t_{subcyc}	
	1	0	0	PSW, TCA reset	
			1		
		1	0		
			1		

Notes: 1. t_{subcyc} = 244.14 µs (when 32.768-kHz crystal oscillator is used)
2. t_{cyc} = 0.9536 µs (when 4.1943-MHz crystal oscillator with 1/4 division is used)
3. Timer counter overflow output period (s) = Input clock period (s) × 256
4. The division ratio must not be modified during time-base mode operation, otherwise an overflow cycle error will occur.

Figure 29 Timer Mode Register A

Timer Mode Register B (TMB: $009): Four-bit write-only register which selects the automatic reloading function, input clock source, and the prescaler division ratio for timer B as shown in figure 30. It is initialized to $0 by MCU reset.

Changes made to TMB are valid from the second instruction cycle after the write instruction is executed. Timer B must be programmed so that it is initialized by a write instruction to timer load register B (TLR) after a mode change becomes valid.



TMB3	Automatic Reloading
0	Disabled
1	Enabled

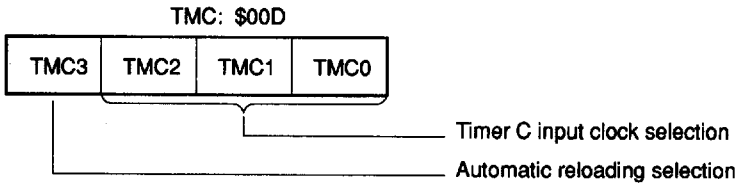
TMB2	TMB1	TMB0	Input Clock Period and Input Clock Source
0	0	0	2048 t_{cyc}
0	0	1	512 t_{cyc}
0	1	0	128 t_{cyc}
0	1	1	32 t_{cyc}
1	0	0	8 t_{cyc}
1	0	1	4 t_{cyc}
1	1	0	2 t_{cyc}
1	1	1	$\overline{INT_1}$ (external event input)

t_{cyc} = 0.9536 µs (when 4.1943-MHz crystal oscillator with 1/4 division is used)

Figure 30 Timer Mode Register B

Timer Mode Register C (TMC: $00D): Four-bit write-only register which selects the automatic reloading function and the prescaler division ratio for timer C as shown in figure 31. It is initialized to $0 by MCU reset.

Changes made to TMC are valid from the second instruction cycle after the write instruction is executed. Timer C must be programmed so that it is initialized by a write instruction to timer load register C (TCR) after a mode change becomes valid.



TMC3	Automatic Reloading
0	Disabled
1	Enabled

TMC2	TMC1	TMC0	Input Clock Period
0	0	0	2048 t_{cyc}
0	0	1	1024 t_{cyc}
0	1	0	512 t_{cyc}
0	1	1	128 t_{cyc}
1	0	0	32 t_{cyc}
1	0	1	8 t_{cyc}
1	1	0	4 t_{cyc}
1	1	1	2 t_{cyc}

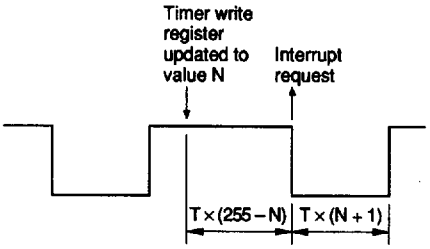
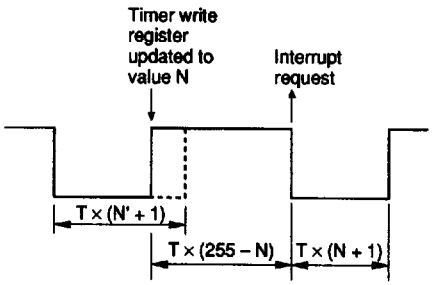
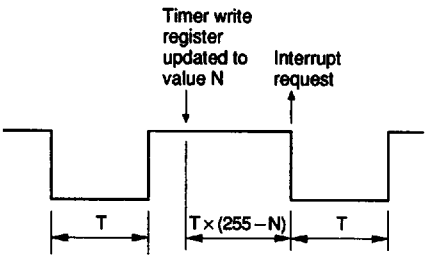
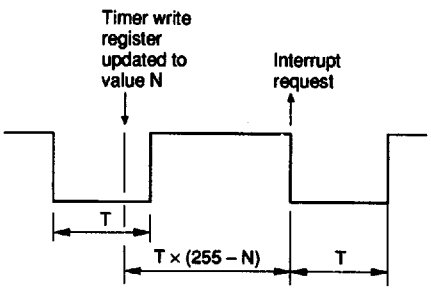
t_{cyc} = 0.9536 µs (when 4.1943-MHz crystal oscillator with 1/4 division is used)

Figure 31 Timer Mode Register C

Notes on Use

When using the timer output as variable-duty pulse output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the variable-duty pulse output differs from the period and duty settings, as shown in table 25. The variable-duty pulse output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the variable-duty pulse output will have the set period and duty cycle.

Table 25 Variable-Duty Pulse Output Following Update of Timer Write Register

Mode	Variable-Duty Pulse Output: Timer Write Register is Updated during High Variable-Duty Pulse Output	Variable-Duty Pulse Output: Timer Write Register is Updated during Low Variable-Duty Pulse Output
Free running		
Reload		

Serial Interface

The MCU has two clock-synchronous serial interfaces. Serial interface 1 transmits and receives 8-bit data, and serial interface 2 transmits and receives 8- or 16-bit data.

Serial Interface 1: Used to serially transmit and receive 8-bit data. It consists of serial 1 data register (S1R), serial mode register A (SMRA), port mode register A (PMRA), an octal counter, and a multiplexer as shown in figure 32. The $R4_0/\overline{SCK_1}$ pin and the transmit clock are controlled by writing data to SMRA. The transmit clock shifts the contents of S1R, which can be read and written to by software, and then transmission starts between two MCUs.

Serial interface 1 is activated by the STS instruction. The octal counter is reset to $0 by the STS instruction, it starts counting at the falling edge of the transmit clock ($\overline{SCK_1}$), and it increments at the rising edge of the clock. When the eighth transmit clock signal is input (serial interface 1 is reset) or when serial transmission is discontinued (octal counter is reset), the serial 1 interrupt request flag (IFS1) is set.

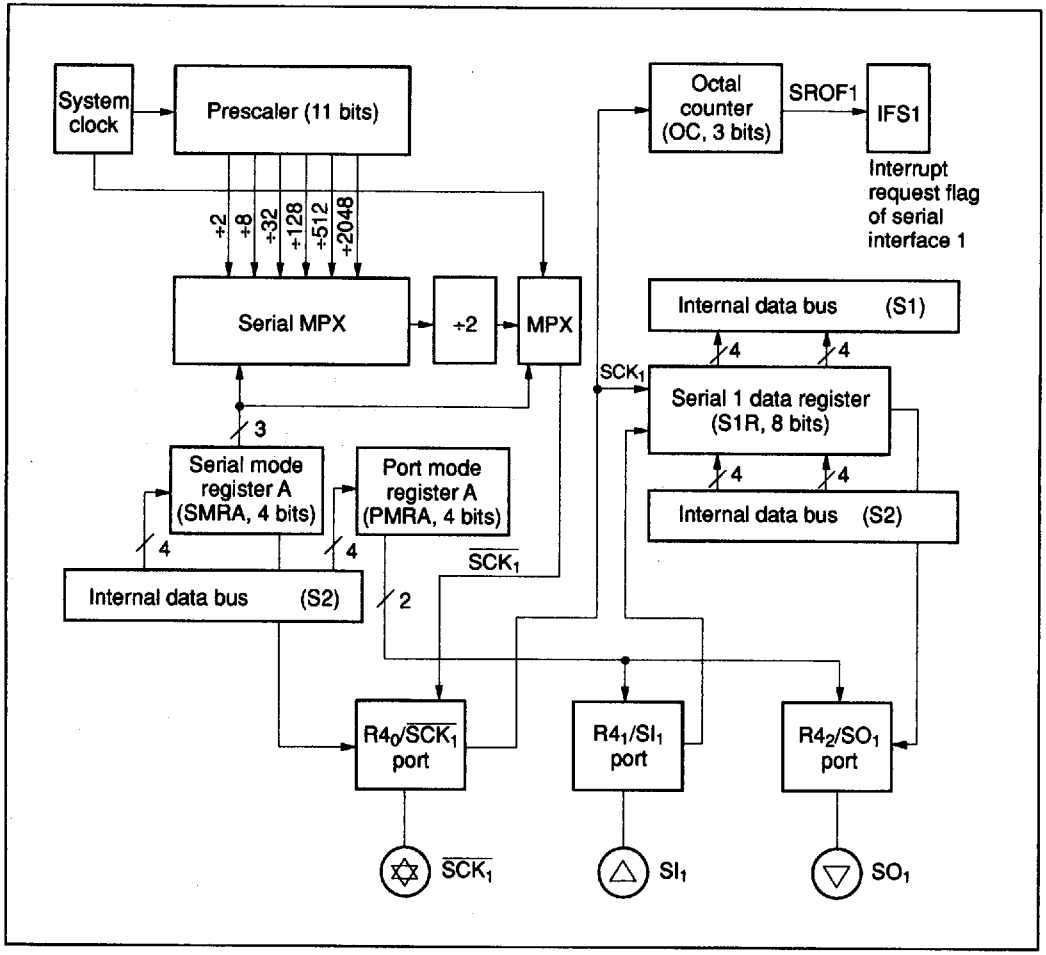
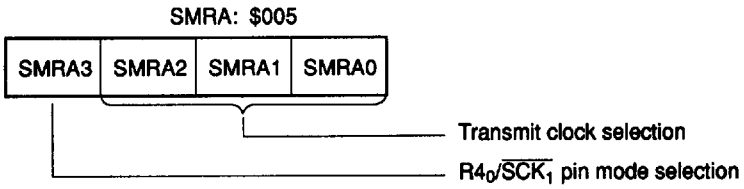


Figure 32 Serial Interface 1 Block Diagram

Serial Mode Register A (SMRA: $005): Four-bit write-only register which controls the $R4_0/\overline{SCK_1}$ pin, transmit clock, and prescaler division ratio for serial interface 1 as shown in figure 33. Writing to SMRA initializes serial interface 1.

A write signal input to SMRA discontinues the input of the transmit clock to the serial 1 data register (S1R) and octal counter. Therefore, if a write occurs during data transmission, the octal counter is reset to $0 to stop transmission, and, at the same time, the serial 1 interrupt request flag (IFS1) is set.

Written data is valid from the second instruction execution cycle after the write. The STS instruction must be executed at least after two cycles. SMRA is initialized to $0 by MCU reset.



SMRA3	$R4_0/\overline{SCK_1}$ Pin
0	$R4_0$ port input/output pin
1	$\overline{SCK_1}$ input/output pin

			Transmit Clock			
SMRA2	SMRA1	SMRA0	$R4_0/\overline{SCK_1}$ Pin	Clock Source	Prescaler Division Ratio	Transmit Clock Period
0	0	0	$\overline{SCK_1}$ output	Prescaler	÷ 2048	4096 t_{cyc}
0	0	1	$\overline{SCK_1}$ output	Prescaler	÷ 512	1024 t_{cyc}
0	1	0	$\overline{SCK_1}$ output	Prescaler	÷ 128	256 t_{cyc}
0	1	1	$\overline{SCK_1}$ output	Prescaler	÷ 32	64 t_{cyc}
1	0	0	$\overline{SCK_1}$ output	Prescaler	÷ 8	16 t_{cyc}
1	0	1	$\overline{SCK_1}$ output	Prescaler	÷ 2	4 t_{cyc}
1	1	0	$\overline{SCK_1}$ output	System clock		1 t_{cyc}
1	1	1	$\overline{SCK_1}$ input	External clock		

Notes: 1. t_{cyc} = 0.9536 µs (when 4.1943-MHz crystal oscillator with 1/4 division ratio is used)
2. When using the $R4_0/\overline{SCK_1}$ pin as pin $R4_0$, do not set SMRA2–SMRA0 to 111 ($\overline{SCK_1}$ input).

Figure 33 Serial Mode Register A

Serial 1 Data Register (S1RL: $006, S1RU: $007): Eight-bit read/write register separated into lower and upper digits located at sequential addresses. Data in this register is output from the SO_1 pin LSB first, in synchronism with the falling edge of the transmit clock, and data is input LSB first to the SI_1 pin at the rising edge of the transmit clock. The input/output timing is shown in figure 34.

Data cannot be read or written during serial data transmission. If data is read or written during transmission, it cannot be guaranteed.

Selecting and Changing Operating Modes: The operating modes of serial interface 1 are shown in table 26. The combination of port mode register A (PMRA) and serial mode register A (SMRA) must be specified as shown in the table. To change the operating mode of serial interface 1, internally initialize serial interface 1 by writing to SMRA.

Table 26 Operating Modes of Serial Interface 1

SMRA	PMRA		
Bit 3	Bit 1	Bit 0	Operating Mode
1	0	0	Continuous clock output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/receive mode

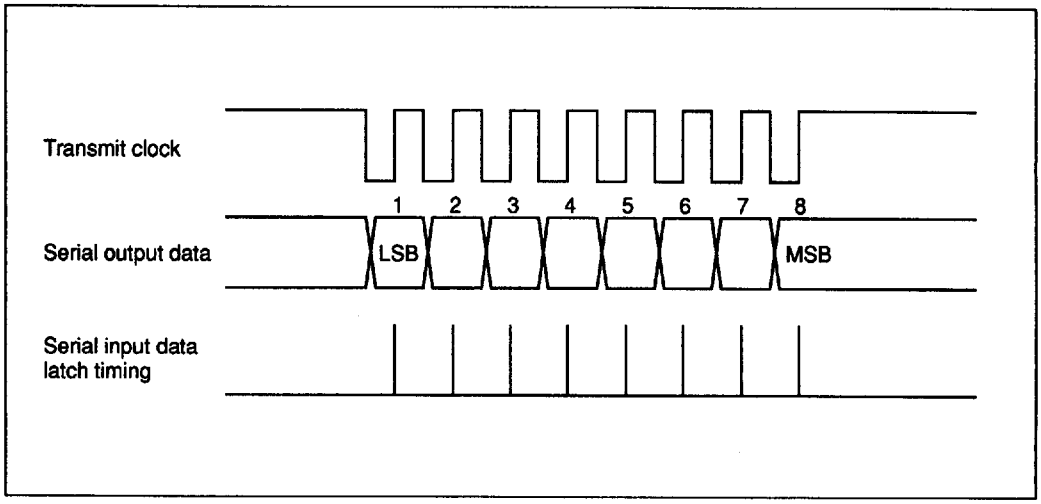


Figure 34 Serial Interface 1 Timing

Serial Interface 1 Operation: Three operating modes are provided for serial interface 1; transitions between them are shown in figure 35.

In STS wait state, serial interface 1 is initialized and the transmit clock is ignored. If the STS instruction is then executed, serial interface 1 enters transmit clock wait state.

In transmit clock wait state, input of the transmit clock increments the octal counter, shifts the serial 1 data register (S1R), and starts serial transmission. However, note that if continuous clock output mode is selected, the transmit clock is continuously output, but data is not transmitted.

During transmission, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and serial interface 1 enters transmit clock wait state. At that point, the serial 1 interrupt flag is set. In this state, if the internal clock has been selected, serial transmission is stopped after the eighth clock is output.

If port mode register A (PMRA) is written to in transmit clock wait state or during transmission, serial mode register A (SMRA) must be written to in oder to initialize serial interface 1, after which serial interface 1 enters the STS wait state.

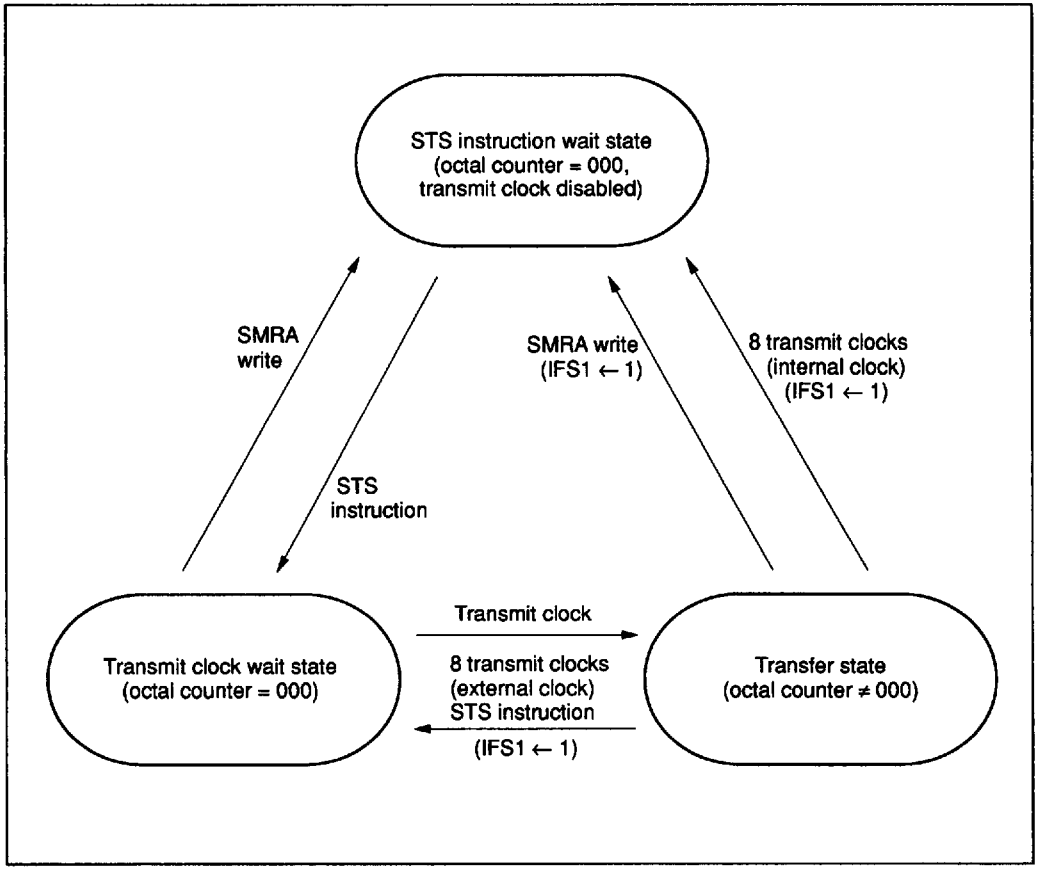


Figure 35 Serial Interface 1 Mode Transitions

Transmit Clock Error Detection: Serial interface 1 will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during transmission. A transmit clock error of this type can be detected as shown in figure 36.

If more than eight transmit clocks are input in transmit clock wait state, serial interface 1's state changes to transfer state, transmit clock wait state, and then back to transfer state.

When serial interface 1 is set to STS wait state by writing data to SMRA at transfer state after the serial 1 interrupt request flag (IFS1) is reset, the flag is set again.

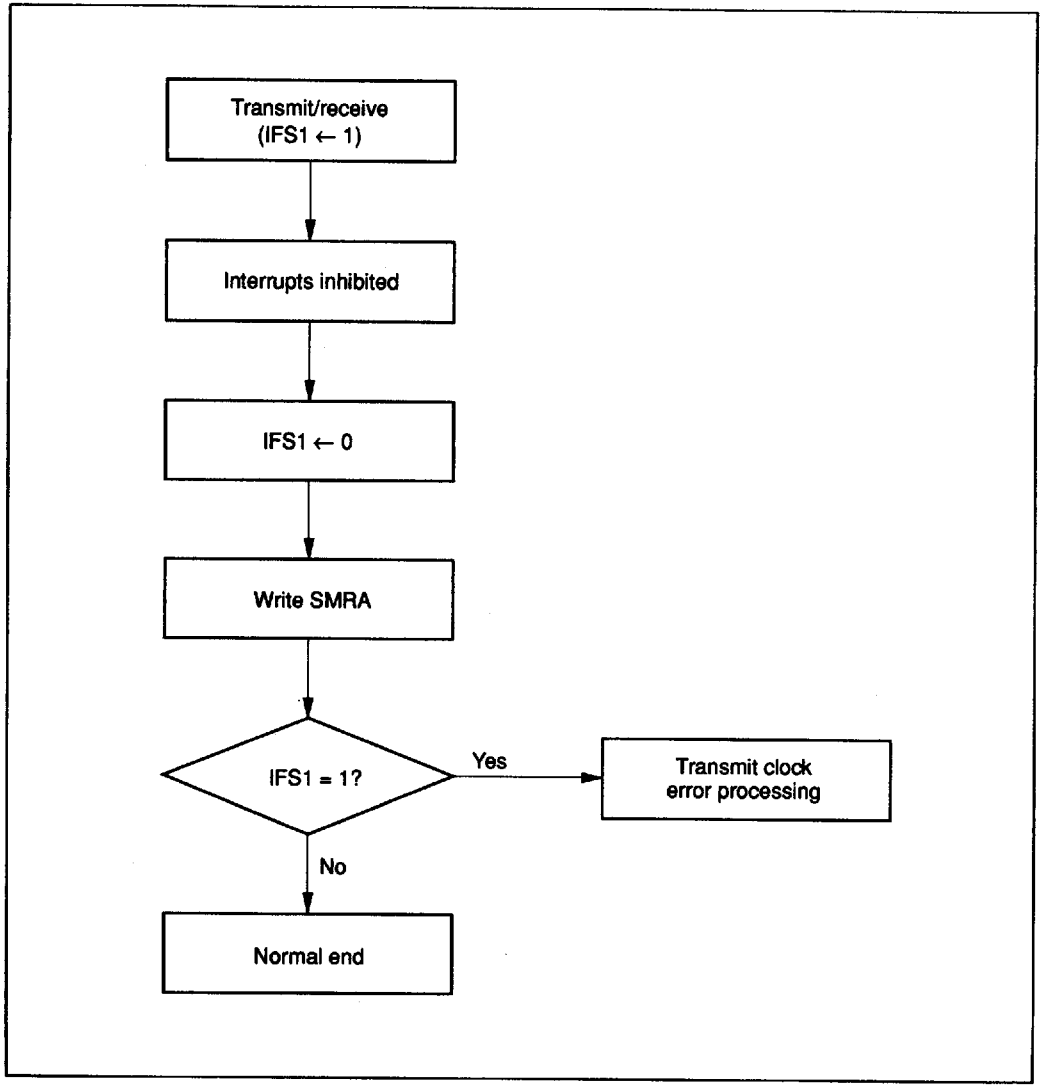


Figure 36 Transmit Clock Error Detection

Serial Interface 2: Used to serially transmit and receive 8- or 16-bit data. It consists of a serial 2 data register (S2R), serial mode register B (SMRB), port mode register C (PMRC), miscellaneous register 2 (MIS2), octal/hexadecimal counter, and multiplexer as shown in figure 37. The $R7_1/\overline{SCK_2}$ pin and the transmit clock are controlled by writing data to SMRB. The transmit clock shifts the contents of the S2R, which can be read and written to by software, and then transmission starts between two MCUs.

Serial interface 2 is activated by a dummy read instruction for SMRB. The octal/hexadecimal counter is reset to $0 by the dummy read instruction for SMRB, it starts counting at the falling edge of the transmit clock ($\overline{SCK_2}$), and it increments at the rising edge of the clock. When the eighth or sixteenth transmit clock signal is input (serial interface 2 is reset) or when serial transmission is discontinued (octal/hexadecimal counter is reset), the serial 2 interrupt request flag (IFS2) is set.

To initiate serial interface 2 by the SMRB dummy read, use a compare instruction on SMRB and the accumulator to read the SMRB. Note that 0000 is read when write-only register SMRB is accessed.

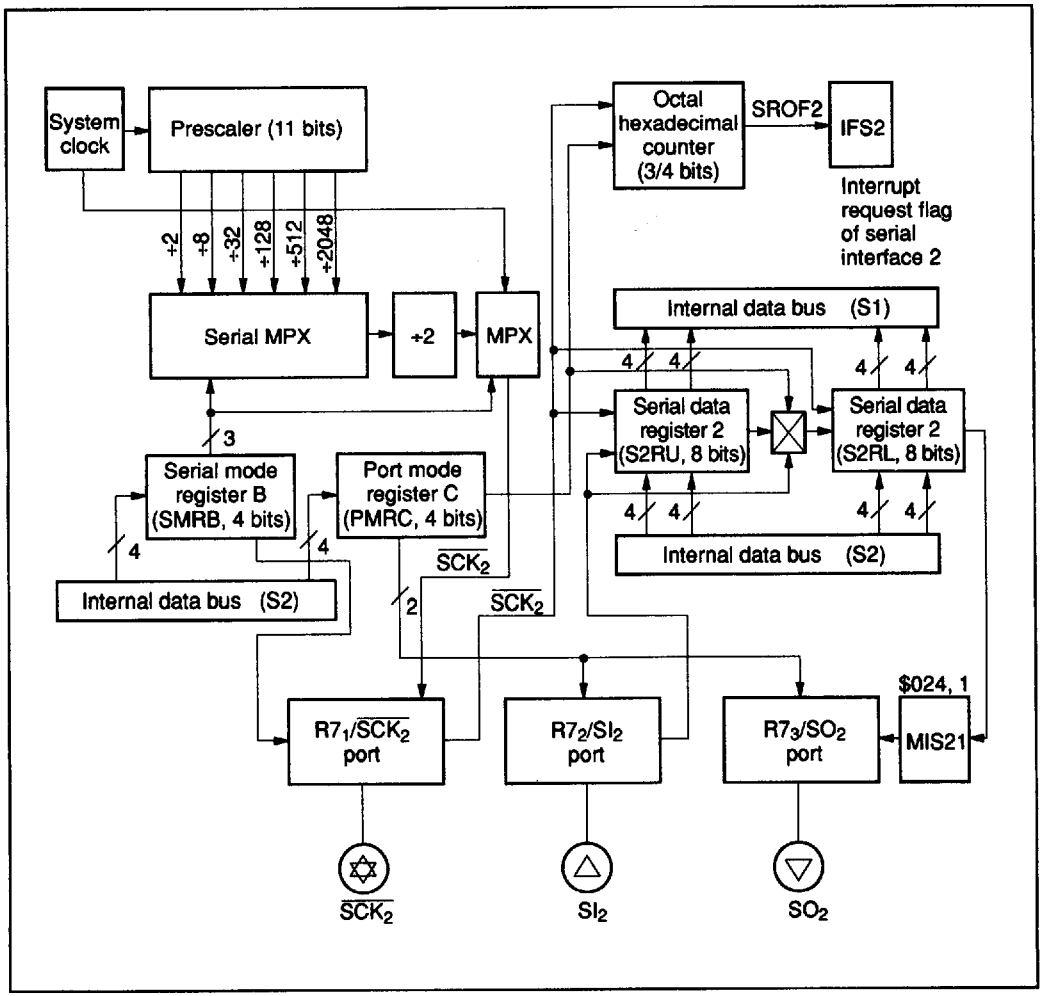
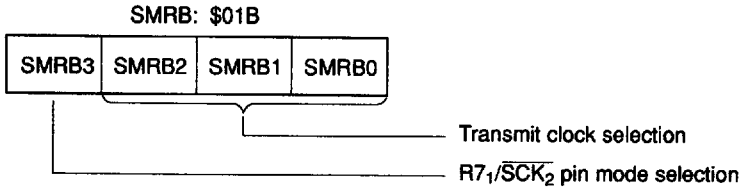


Figure 37 Serial Interface 2 Block Diagram

Serial Mode Register B (SMRB: $01B): Four-bit write-only register which controls the $R7_1/\overline{SCK_2}$ pin, transmit clock, and prescaler division ratio as shown in figure 38. Writing to SMRB initializes serial interface 2.

A write signal input to SMRB discontinues the input of the transmit clock to the serial 2 data register (S2R) and octal/hexadecimal counter. Therefore, if a write occurs during data transmission, the octal/hexadecimal counter is reset to $0 to stop transmission, and, at the same time, the serial 2 interrupt request flag (IFS2) is set.

Written data is valid from the second instruction execution cycle after the write. The SMRB dummy read must be executed after at least two cycles. SMRB is initialized to $0 by MCU reset.



SMRB3	$R7_1/\overline{SCK_2}$
0	$R7_1$ port input/output pin
1	$\overline{SCK_2}$ input/output pin

			Transmit Clock			
SMRB2	SMRB1	SMRB0	$R7_1/\overline{SCK_2}$ Pin	Clock Source	Prescaler Division Ratio	Transmit Clock Period
0	0	0	$\overline{SCK_2}$ output	Prescaler	÷ 2048	4096 t_{cyc}
0	0	1	$\overline{SCK_2}$ output	Prescaler	÷ 512	1024 t_{cyc}
0	1	0	$\overline{SCK_2}$ output	Prescaler	÷ 128	256 t_{cyc}
0	1	1	$\overline{SCK_2}$ output	Prescaler	÷ 32	64 t_{cyc}
1	0	0	$\overline{SCK_2}$ output	Prescaler	÷ 8	16 t_{cyc}
1	0	1	$\overline{SCK_2}$ output	Prescaler	÷ 2	4 t_{cyc}
1	1	0	$\overline{SCK_2}$ output	System clock		1 t_{cyc}
1	1	1	$\overline{SCK_2}$ input	External clock		

Notes: 1. t_{cyc} = 0.9536 µs (when 4.1943-MHz crystal oscillator with 1/4 division ratio is used)
2. When using the $R7_1/\overline{SCK_2}$ pin as pin $R7_1$, do not set SMRB3–SMRB0 to 111 ($\overline{SCK_2}$ input).

Figure 38 Serial Mode Register B

Serial 2 Data Register (S2RLL: $01C, S2RLU: $01D, S2RUL: $01E, S2RUU: $01F): Sixteen-bit read/write register separated into two lower and two upper digits located at sequential addresses. Data in this register is output from the SO_2 pin LSB first, in synchronism with the falling edge of the transmit clock, and data is input LSB first to the SI_2 pin at the rising edge of the transmit clock. The input/output timing is shown in figure 39.

Data cannot be read or written during serial data transmission. If data is read or written during transmission, it cannot be guaranteed.

Miscellaneous Register 2 (MIS2: $024): Bit 1 of MIS2 is connected to the final output circuit of the serial 2 data register (S2R).

The value of the SO_2 pin can be changed by controlling bit 1 of MIS2 in transmit mode after the completion of transmission. If bit 1 is written to, all other bits must be set to 0. If bit 1 is not written to, SO_2 continues to output the value of the last bit to be transmitted.

Selecting and Changing Operating Mode: Table 27 lists serial interface 2's operating modes. Specify the operating mode and data length (8- or 16-bit) by a combination of PMRC and SMRB values. To change the operating mode of serial interface 2, internally initialize serial interface 2 by writing to SMRB.

Table 27 Operating Modes of Serial Interface 2

SMRB	PMRC			
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	0	Continuous clock output mode
1	0	0	1	8-bit transmit mode
1	0	1	0	8-bit receive mode
1	0	1	1	8-bit transmit/receive mode
1	1	0	0	Continuous clock output mode
1	1	0	1	16-bit transmit mode
1	1	1	0	16-bit receive mode
1	1	1	1	16-bit transmit/receive mode

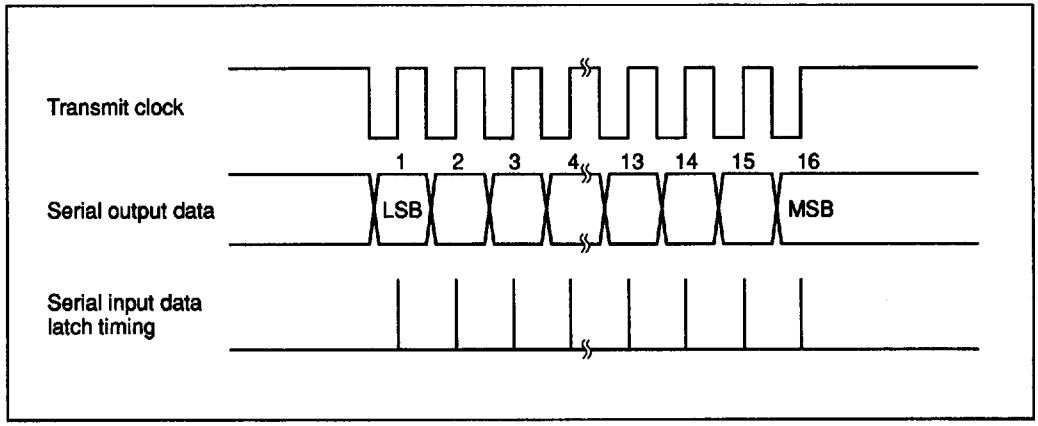


Figure 39 Serial Interface 2 Timing

Serial Interface 2 Operation: Three operating modes are provided for serial interface 2; transitions between them are shown in figure 40.

In serial 2 start wait state, serial interface 2 is initialized and the transmit clock is ignored. If an SMRB dummy read is executed, serial interface 2 enters transmit clock wait state.

In transmit clock wait state, input of the transmit clock increments the octal/hexadecimal counter, shifts the serial 2 data register (S2R), and starts serial transmission. However, note that if continuous clock output mode is selected, the transmit clock is continuously output, but data is not transmitted.

During transmission, the input of eight or sixteen clocks or a SMRB dummy read sets the octal/hexadecimal counter to 000/0000, and serial interface 2 enters transmit clock wait state. At that point, the serial 2 interrupt flag is set. In this state, if the internal clock has been selected, serial transmission is stopped after the eighth or sixteenth clock is output.

If port mode register C (PMRC) is written to in transmit clock wait state or during transmission, SMRB must be written to in order to initialize serial interface 2, after which serial interface 2 enters serial 2 start wait state.

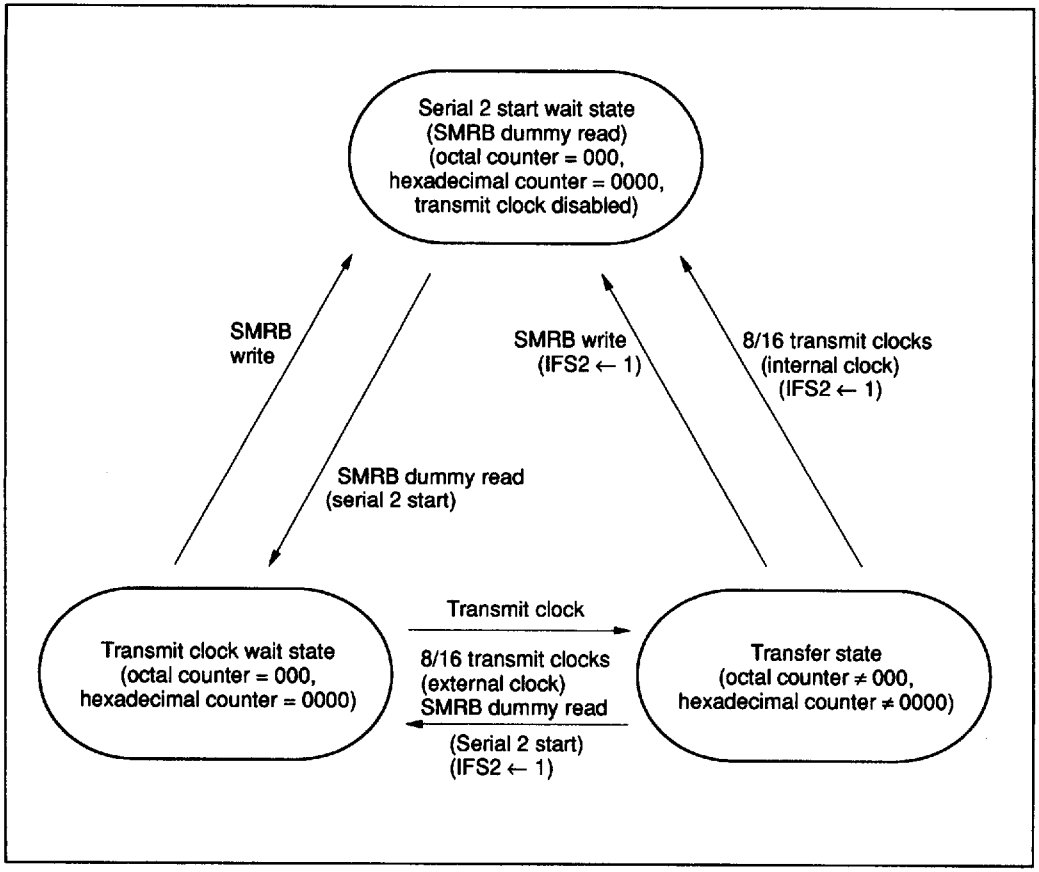


Figure 40 Serial Interface 2 Mode Transitions

Transmit Clock Error Detection: Serial interface 2 will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during transmission. A transmit clock error of this type can be detected as shown in figure 41.

If more than eight or sixteen transmit clocks are input in transmit clock wait state, serial interface 2's state changes to transfer state, transmit clock wait state, then back to transfer state.

When serial interface 2 is set to serial 2 start wait state by writing data to SMRB at transfer state after the serial interface 2 interrupt request flag (IFS2) is reset, the flag is set again.

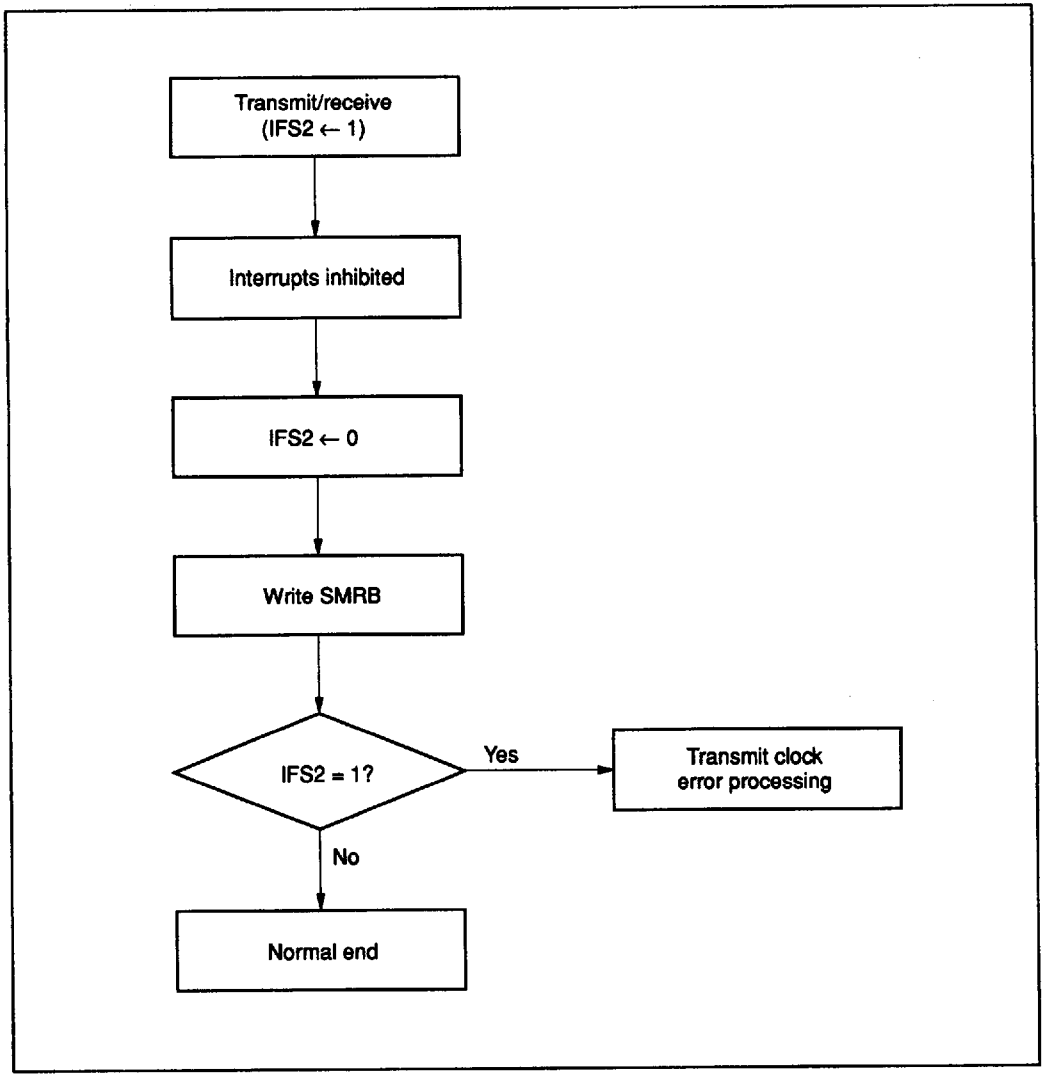


Figure 41 Transmit Clock Error Detection

Vacuum Fluorescent Display (VFD) Controller

The MCU has a VFD controller that can control 16 digit pins and 16 segment pins, and a high-voltage, high-current driver which enables VFD display (figure 42). The controller consists of VFD data RAM, a VFD control register (VCR), a dimmer mode register (DMR), and a display timing generator. The display driver consists of 32 high-voltage, high-current pins, a VFD segment register (FSR), and a VFD digit register (FDR), and can specify display formats from 8 segments × 2 digits to 16 segments × 16 digits.

One display timing frame is divided into 17 periods. During one of 17 periods, the pin selected by the VFD segment/digit register can be used for key scanning. When key scanning is enabled, the CPU can control all the segment/digit pins as a D port or R port.

An example of the connection between the MCU and the VFD is shown in figure 43.

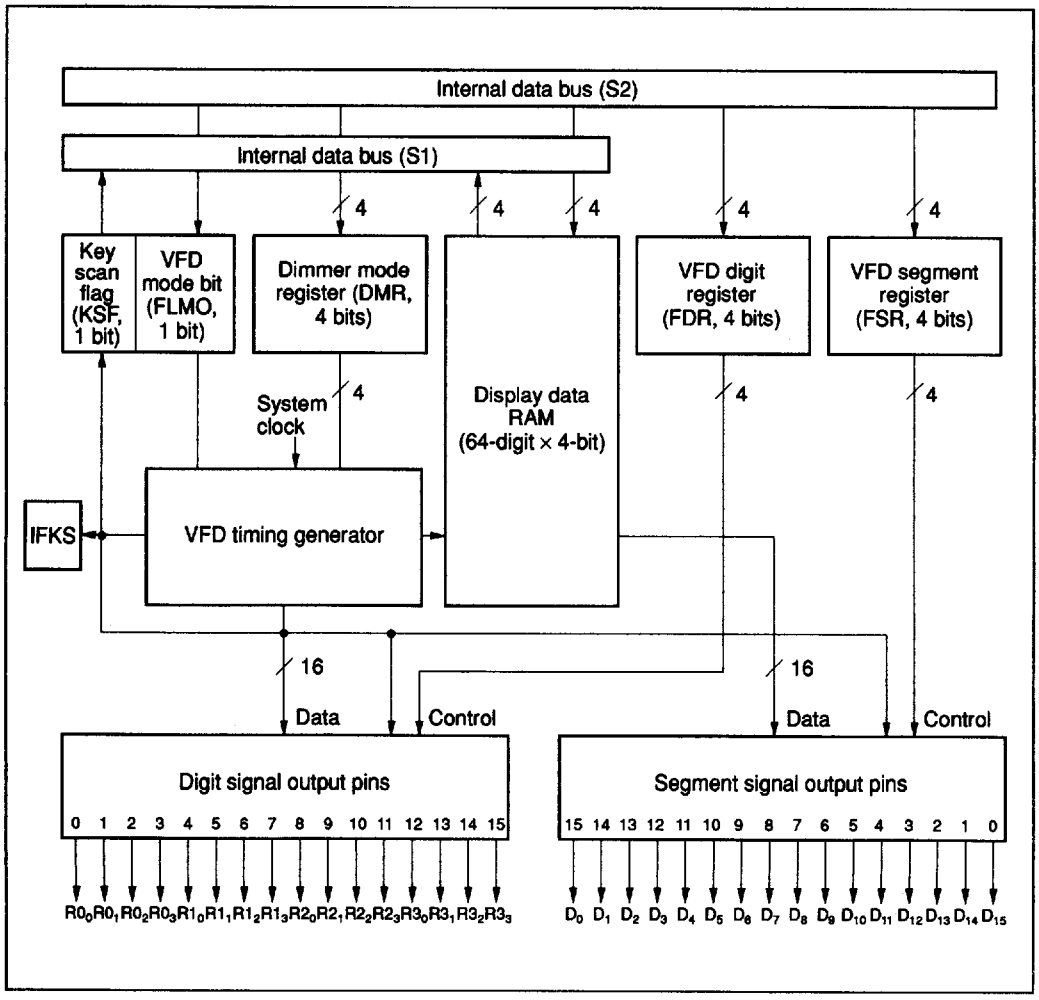


Figure 42 VFD Controller Block Diagram

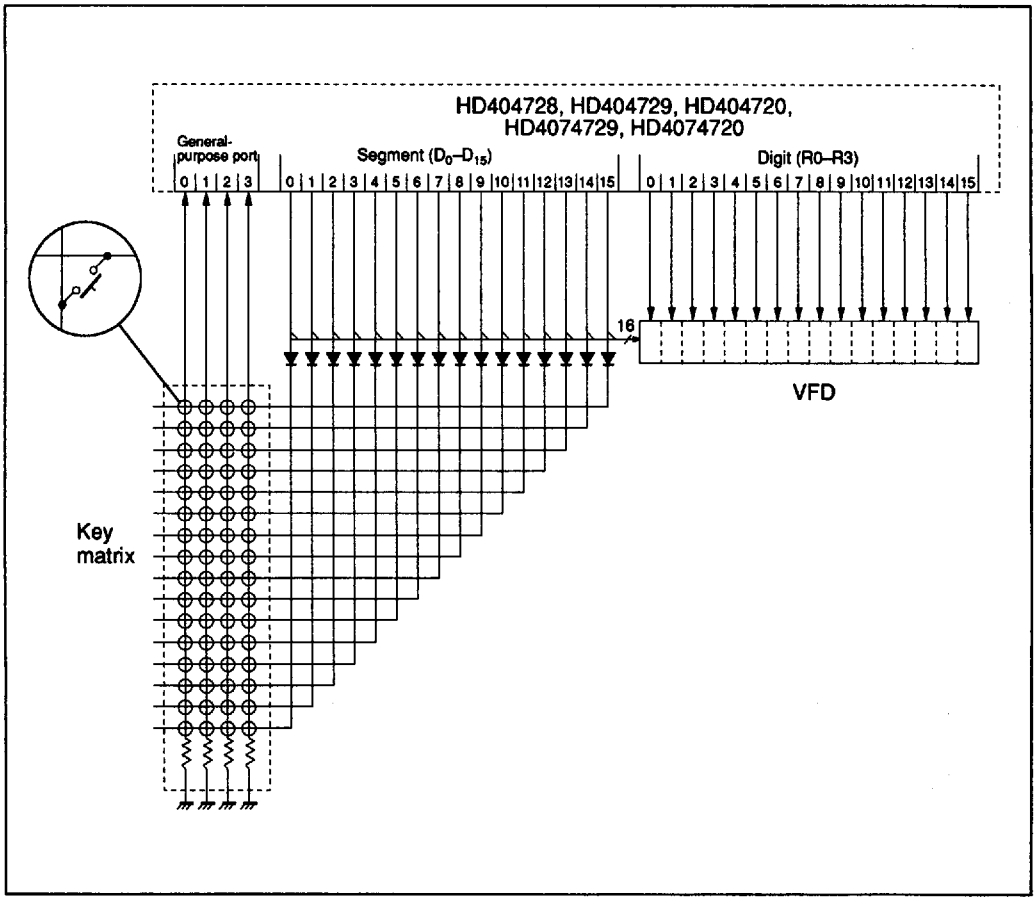


Figure 43 Example of VFD Connection

VFD Data RAM: Addresses in VFD data RAM are listed in table 28. RAM area that is not used in display mode can be assigned for general purposes.

Table 28 VFD Data RAM Addresses

Pin	Segment / Digit	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$R0_0$	0	$090				$080				$070					$060		
$R0_1$	1	$091				$081				$071					$061		
$R0_2$	2	$092				$082				$072					$062		
$R0_3$	3	$093				$083				$073					$063		
$R1_0$	4	$094				$084				$074					$064		
$R1_1$	5	$095				$085				$075					$065		
$R1_2$	6	$096				$086				$076					$066		
$R1_3$	7	$097				$087				$077					$067		
$R2_0$	8	$098				$088				$078					$068		
$R2_1$	9	$099				$089				$079					$069		
$R2_2$	10	$09A				$08A				$07A					$06A		
$R2_3$	11	$09B				$08B				$07B					$06B		
$R3_0$	12	$09C				$08C				$07C *					$06C *		
$R3_1$	13	$09D				$08D				$07D *					$06D *		
$R3_2$	14	$09E				$08E				$07E *					$06E *		
$R3_3$	15	$09F				$08F				$07F *					$06F *		

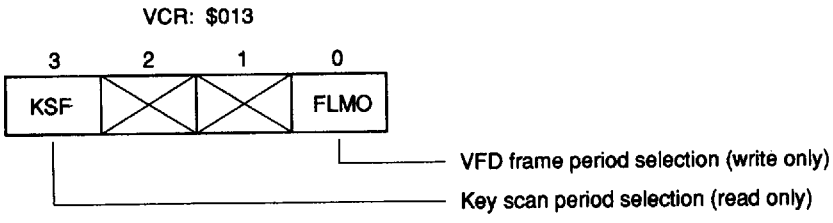
Notes: * The contents of RAM addresses $07C–$07F and $06C–$06F (not display data) are output from segment pins at the timing set by digits 12–15.

1. In each segment, the right end corresponds to the LSB and the left end to the MSB.
2. Shading indicates the VFD data RAM locations used in displaying 8-segment × 12-digit data. In this example, other locations can be used for general purposes.

VFD Control Register (VCR: $013): The VFD control register consists of a 1-bit write-only register and a 1-bit read-only/RAM bit test register (figure 44).

The VFD mode bit (FLMO: $013, bit 0) is a write-only bit which selects a frame period of either 3264- or 6528-instruction cycles. This bit is initialized to 0 by MCU reset.

The key scan flag (KSF: $013, bit 3) is a read/test flag which indicates either the display period or the key scan period. The key scan period is 1/17 of the frame period. During the key scan period, the D port and R0–R3 ports are used as CPU-controlled general-purpose ports, and key scan can be enabled by software. At the rising edge of the KSF, the key scan interrupt request flag (IFKS) is set to 1.



VCR

Bit 3	Period
0	Display period
1	Key scan period

VCR

Bit 0	T_{frame}: Frame Period		T_{digit}: Key Scan Digit Period		T_{dimmer}: Dimmer Resolution	
0	6528 t_{cyc}	6226 µs*	384 t_{cyc}	366.2 µs*	24 t_{cyc}	22.89 µs*
1	3264 t_{cyc}	3113 µs*	192 t_{cyc}	183.1 µs*	12 t_{cyc}	11.44 µs*

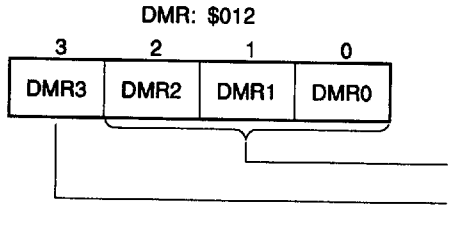
Note: * t_{cyc} = 0.9536 µs (when 4.1943-MHz crystal oscillator with 1/4 division ratio is used)

Figure 44 VFD Control Register

Dimmer Mode Register (DMR: $012): Four-bit write-only register which controls the VFD driver pin mode and a digit signal output waveform (figure 45). Eight waveforms can be selected. The DMR is initialized to $0 by MCU reset.

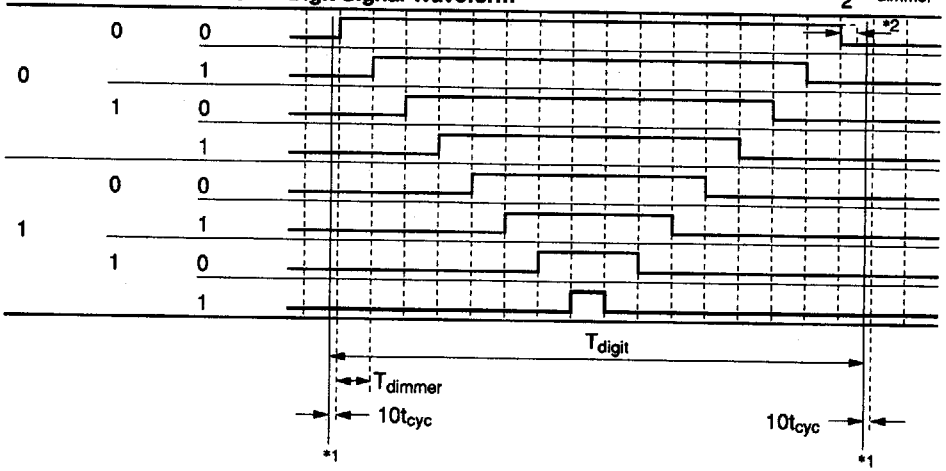
For details of digit waveform resolution, refer to the VFD Control Register section since resolution is affected by the VFD mode register.

DMR3 functions as a master enable bit for the VFD controller. While DMR3 is 0, the D_0–D_{15} and R0–R3 ports are used as general-purpose ports, and the display timing generator remains reset.



DMR Bit 3	D_0–D_{15} and R0–R3 Mode
0	General purpose ports
1	VFD driver, depending on the status of FDR and FSR

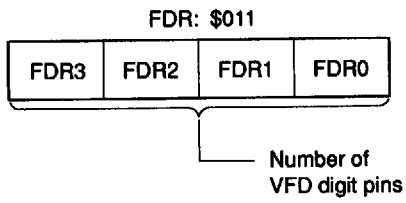
DMR Bit 2	DMR Bit 1	DMR Bit 0	Digit Signal Waveform
0	0	0	
		1	
	1	0	
		1	
1	0	0	
		1	
	1	0	
		1	

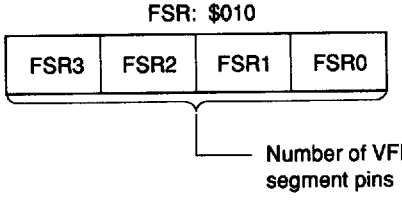


Notes: 1. This is the timing of the segment signal. For details of T_{digit} and T_{dimmer}, refer to the VFD Control Register section.
2. When VCR bit 0 is 0 and DMR is $8, the high level width of the digit signal wave is 15.5 T_{dimmer} cycles.

Figure 45 Dimmer Mode Register

VFD Digit Register (FDR: $011), VFD Segment Register (FSR: $010): Four-bit write-only registers which control the VFD driver pins (figure 46). The pins not selected by these registers are used for general purposes. The pins selected by these registers are used for the VFD driver or general purposes, depending on the state of bit 3 of the DMR and the key scan flag. FDR and FSR are initialized to $0 by MCU reset.





FDR 3 2 1 0	Number of Digits	Digit Signal Output Pins
0 0 0 0	0	None
0 0 0 1	2	$FD_0/R0_0$–$FD_1/R0_1$
0 0 1 0	3	$FD_0/R0_0$–$FD_2/R0_2$
0 0 1 1	4	$FD_0/R0_0$–$FD_3/R0_3$
0 1 0 0	5	$FD_0/R0_0$–$FD_4/R1_0$
0 1 0 1	6	$FD_0/R0_0$–$FD_5/R1_1$
0 1 1 0	7	$FD_0/R0_0$–$FD_6/R1_2$
0 1 1 1	8	$FD_0/R0_0$–$FD_7/R1_3$
1 0 0 0	9	$FD_0/R0_0$–$FD_8/R2_0$
1 0 0 1	10	$FD_0/R0_0$–$FD_9/R2_1$
1 0 1 0	11	$FD_0/R0_0$–$FD_{10}/R2_2$
1 0 1 1	12	$FD_0/R0_0$–$FD_{11}/R2_3$
1 1 0 0	13	$FD_0/R0_0$–$FD_{12}/R3_0$
1 1 0 1	14	$FD_0/R0_0$–$FD_{13}/R3_1$
1 1 1 0	15	$FD_0/R0_0$–$FD_{14}/R3_2$
1 1 1 1	16	$FD_0/R0_0$–$FD_{15}/R3_3$

FSR 3 2 1 0	Number of Segments	Segment Signal Output Pins
0 0 0 0	0	None
0 0 0 1	8	FS_0/D_{15}–FS_7/D_8
0 0 1 0	9	FS_0/D_{15}–FS_8/D_7
0 0 1 1	10	FS_0/D_{15}–FS_9/D_6
0 1 0 0	11	FS_0/D_{15}–FS_{10}/D_5
0 1 0 1	12	FS_0/D_{15}–FS_{11}/D_4
0 1 1 0	13	FS_0/D_{15}–FS_{12}/D_3
0 1 1 1	14	FS_0/D_{15}–FS_{13}/D_2
1 0 0 0	15	FS_0/D_{15}–FS_{14}/D_1
1 0 0 1	16	FS_0/D_{15}–FS_{15}/D_0
1 0 1 0	Not used	
1 0 1 1		
1 1 0 0		
1 1 0 1		
1 1 1 0		
1 1 1 1		

Figure 46 VFD Digit Register and Segment Register

Pulse Width Modulator (PWM)

The MCU's 14-bit PWM can be used as a 14-bit D/A converter by externally connecting a low-pass filter to it. A pulse-division PWM method is used to obtain the resolution and high-speed response required for the voltage synthesizer tuning system.

The features of the PWM are as follows:

- One conversion cycle: $t_{cyc} \times 8192$
- Minimum modulation width: $t_{cyc}/2$
- Pulse-division method for ripple reduction

The PWM has the registers shown in table 29, and a block diagram of the PWM is shown in figure 47.

When data is written to PWM data register 3 (PWDR3), the data is latched into the modulator and a PWM signal is then output in synchronism with the internal clock signal. Note that bits 3 and 2 of PWDR3 are invalid. The PWM operation is shown in figure 48.

Table 29 PWM Data Registers

Register Name	Bit Count	Read/Write
PWM data register 3 (PWDR3: $019)	2	Write
PWM data register 2 (PWDR2: $018)	4	Write
PWM data register 1 (PWDR1: $017)	4	Write
PWM data register 0 (PWDR0: $016)	4	Write

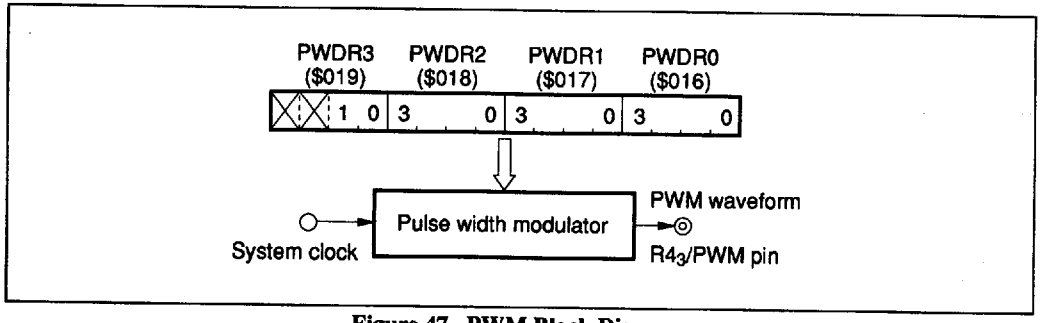


Figure 47 PWM Block Diagram

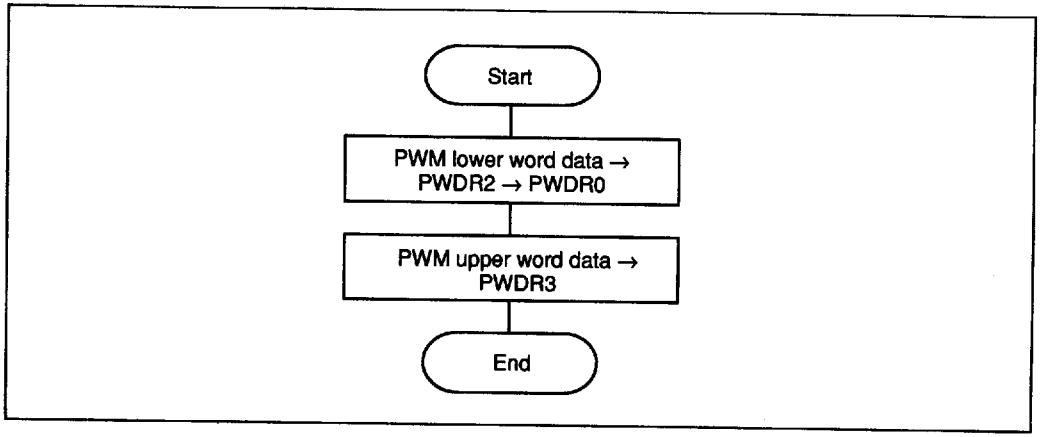
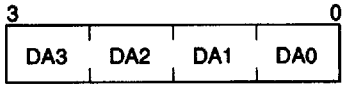


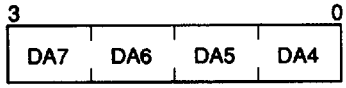
Figure 48 PWM Operation

PWM Registers

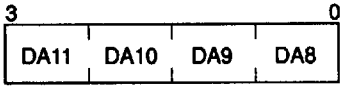
PWM Data Register 0 (PWDR0: $016): Four-bit write-only register.



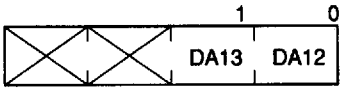
PWM Data Register 1 (PWDR1: $017): Four-bit write-only register.



PWM Data Register 2 (PWDR2: $018): Four-bit write-only register.



PWM Data Register 3 (PWDR3 $019): Two-bit write-only register.



PWM Operation

The PWM waveform shown in figure 49 is output from the PWM pin. One frame period generates 64 clock pulses. The relationship between total pulse width at low level in one frame (T_L) and the data value is given by the following equation.

$$T_L = (\text{data value} + 64) \times \frac{t_{cyc}}{2}$$ (t_{cyc}: instruction execution time)

When f_{OSC} = 4 MHz:
1 conversion cycle = 8192 µs
t_{fn} = 128 µs
$2/f_{OSC}$ (resolution) = 0.5 µs

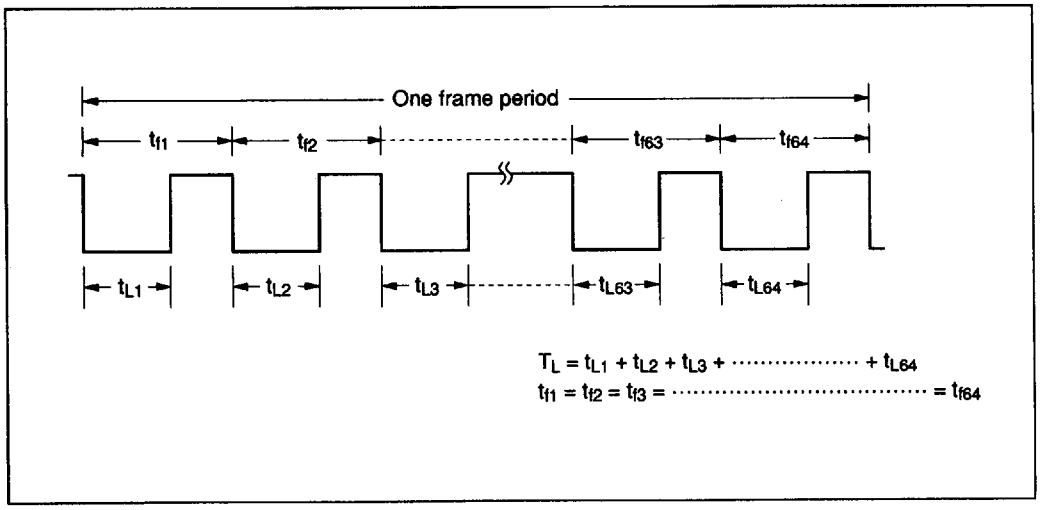


Figure 49 PWM Waveform

Programmable ROM

The HD4074729 and HD4074720 are ZTAT™ microcomputers with built-in PROM that can be programmed in PROM mode.

PROM Mode Pin Description

Pin Number			MCU Mode		PROM Mode		Pin Number			MCU Mode		PROM Mode	
DP-64S DC-64S	FP-64B	FP-64A	Pin Name	I/O	Pin Name	I/O	DP-64S DC-64S	FP-64B	FP-64A	Pin Name	I/O	Pin Name	I/O
1	59	57	D_{11}/FS_4	I/O			33	27	25	$R4_0/\overline{SCK_1}$	I/O	PSEL*	I*
2	60	58	D_{12}/FS_3	I/O			34	28	26	$R4_1/SI_1$	I/O	O_4	I/O
3	61	59	D_{13}/FS_2	I/O			35	29	27	$R4_2/SO_1$	I/O	O_3	I/O
4	62	60	D_{14}/FS_1	I/O			36	30	28	$R4_3$/PWM	I/O	O_2	I/O
5	63	61	D_{15}/FS_0	I/O			37	31	29	$R7_0$/BUZZ	I/O	O_4	I/O
6	64	62	$R0_0/FD_0$	I/O	A_1	I	38	32	30	$R7_1/\overline{SCK_2}$	I/O	O_5	I/O
7	1	63	$R0_1/FD_1$	I/O	A_2	I	39	33	31	$R7_2/SI_2$	I/O	O_6	I/O
8	2	64	$R0_2/FD_2$	I/O	A_3	I	40	34	32	$R7_3/SO_2$	I/O	O_7	I/O
9	3	1	$R0_3/FD_3$	I/O	A_4	I	41	35	33	$R8_0$	I/O	O_1	I/O
10	4	2	$R1_0/FD_4$	I/O	A_5	I	42	36	34	$R8_1$	I/O	O_0	I/O
11	5	3	$R1_1/FD_5$	I/O	A_6	I	43	37	35	$R9_0$	I	V_{PP}	
12	6	4	$R1_2/FD_6$	I/O	A_7	I	44	38	36	$R9_1$	I	A_9	I
13	7	5	$R1_3/FD_7$	I/O	A_8	I	45	39	37	$R9_2$	I	$\overline{M_0}$	I
14	8	6	$R2_0/FD_8$	I/O	A_0	I	46	40	38	$R9_3$	I	$\overline{M_1}$	I
15	9	7	$R2_1/FD_9$	I/O	A_{10}	I	47	41	39	RESET	I	RESET	I
16	10	8	$R2_2/FD_{10}$	I/O	A_{11}	I	48	42	40	OSC_2	O		
17	11	9	$R2_3/FD_{11}$	I/O	A_{12}	I	49	43	41	OSC_1	I		
18	12	10	RA_0	I	V_{CC}		50	44	42	GND		GND	
19	13	11	RA_1/V_{disp}	I			51	45	43	CL_1	I	GND	
20	14	12	$R3_0/FD_{12}$	I/O	A_{13}	I	52	46	44	CL_2	O		
21	15	13	$R3_1/FD_{13}$	I/O	A_{14}	I	53	47	45	$\overline{TEST}$	I	$\overline{TEST}$	I
22	16	14	$R3_2/FD_{14}$	I/O			54	48	46	D_0/FS_{15}	I/O		
23	17	15	$R3_3/FD_{15}$	I/O			55	49	47	D_1/FS_{14}	I/O		
24	18	16	$R5_0$	I/O	$\overline{CE}$	I	56	50	48	D_2/FS_{13}	I/O		
25	19	17	$R5_1$	I/O	$\overline{OE}$	I	57	51	49	D_3/FS_{12}	I/O		
26	20	18	$R5_2$	I/O	V_{CC}		58	52	50	D_4/FS_{11}	I/O		
27	21	19	$R5_3$	I/O	V_{CC}		59	53	51	D_5/FS_{10}	I/O		
28	22	20	$R6_0/\overline{INT_0}$	I/O	O_0	I/O	60	54	52	D_6/FS_9	I/O		
29	23	21	$R6_1/\overline{INT_1}$	I/O	O_1	I/O	61	55	53	D_7/FS_8	I/O		
30	24	22	$R6_2/\overline{INT_2}$	I/O	O_2	I/O	62	56	54	D_8/FS_7	I/O		
31	25	23	$R6_3/\overline{INT_3}$	I/O	O_3	I/O	63	57	55	D_9/FS_6	I/O		
32	26	24	V_{CC}		V_{CC}		64	58	56	D_{10}/FS_5	I/O		

Notes: * Applies to HD4074720S, HD4074720FS and HD4074720C.

1. I/O: Input/output pin, I: Input pin, O: Output pin
2. Each of O_0–O_4 has 2 pins; connect each pair together for use.

PROM Mode Pin Functions

V_{PP}: Applies the programming voltage (12.5 V ± 0.3 V) to the built-in PROM.

$\overline{CE}$: Inputs a control signal to enable PROM programming and verification.

$\overline{OE}$: Inputs a data output control signal for verification.

A_0–A_{14}: Act as address input pins of the built-in PROM.

O_0–O_7: Act as data bus input pins of the built-in PROM.

$\overline{M_0}$, $\overline{M_1}$: Used to set PROM mode. The MCU is set to the PROM mode by pulling $\overline{M_0}$, $\overline{M_1}$, and $\overline{TEST}$ low, and RESET high.

PSEL (HD4074720S, HD4074720FS and HD4074720C): Inputs a signal which selects the program ROM (16,384 words) or pattern ROM (8,192 words).

PSEL	PROM Select
0	Program ROM (16,384 words)
1	Pattern ROM (8,192 words)

Programming the Built-in PROM

The MCU's built-in PROM is programmed in PROM mode which is set by pulling $\overline{TEST}$, $\overline{M_0}$, and M_1 low, and RESET high, as shown in figure 50. In PROM mode, the MCU does not operate, but the 16-kword PROM and 8-kword PROM (HD4074720) can both be programmed in the same way as any other commercial 27256 EPROM using a standard PROM programmer and a 64-to-28-pin socket adapter. Recommended PROM programmers and socket adapters are listed in table 31. For HD4074720, these socket adapters have PSEL select switches, which select the 16-kword PROM or 8-kword PROM by setting PSEL low or high.

Since an HMCS400-series instruction is ten bits long, the HMCS400-series MCU has a built-in conversion circuit to enable use of a general-purpose PROM programmer. This circuit splits each instruction into a lower 5 bits and an upper 5 bits that are read from or written to consecutive addresses, as shown in figure 51. This means that if, for example, a 16-kword built-in PROM is to be programmed by a general-purpose PROM programmer, a 32-kbyte address space ($0000–$7FFF) must be specified.

Programming and Verification: The built-in PROM of the MCU can be programmed at high-speed programming sequence without risk of voltage stress or damage to data reliability.

Programming and verification modes are selected as shown in table 30, and the memory map in PROM mode is shown in figure 51.

For details of PROM programming, refer to the Notes on PROM Programming section.

Warnings

1. Always specify addresses $0000 to $7FFF when programming with a PROM programmer. For 8-kword PROM, the data in addresses $4000 to $7FFF must be $FF. If address $8000 ($4000 in the 8-kword PROM) or higher is accessed in the 16-kword PROM, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.

   Note that the plastic-package version cannot be erased and reprogrammed, but the ceramic window-package version can be reprogrammed after being exposed to ultraviolet light.

2. Make sure that the PROM programmer, socket adapter, and LSI are aligned correctly (their pin 1 positions match), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed onto the programmer.

3. PROM programmers have two voltages (V_{PP}): 12.5 V and 21 V. Remember that ZTAT™ devices require a V_{PP} of 12.5 V—the 21-V setting will damage them. A voltage of 12.5 V is the Intel's 27256 setting.

Erasure (Window Package)

Data in the PROM is erased by exposing the LSI to ultraviolet light of wavelength 2537 Å for an integrated dose of at least 15 W·s/cm^2. These conditions can be satisfied by placing the LSI about 2–3 cm away from an ultraviolet lamp with a rating of 12,000 μW/cm^2 for about 20 minutes. After erasure, all PROM bits are set to 1.

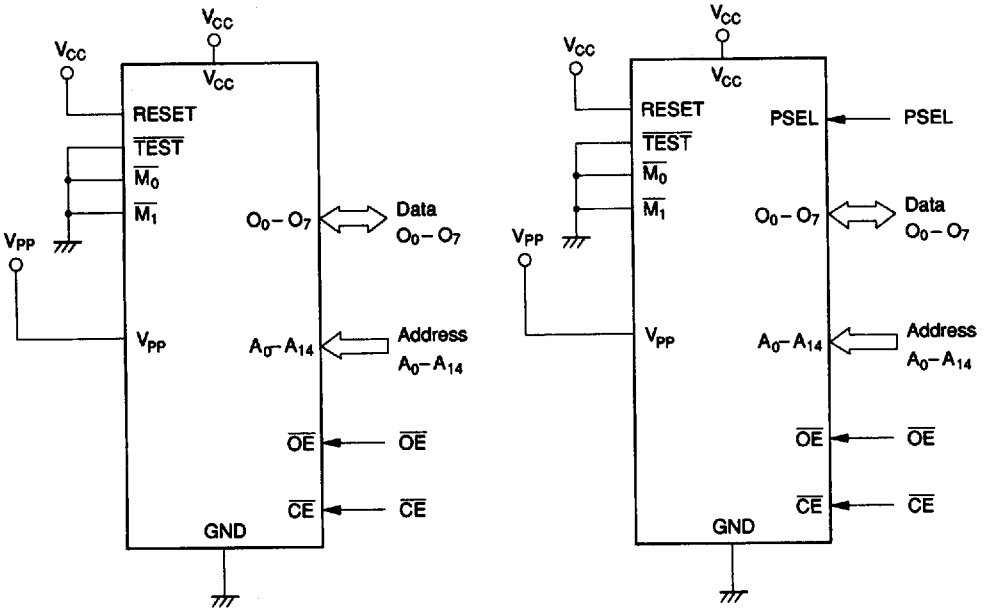
For details of packages with windows, refer to the Notes on Window Packages section.

Table 30 PROM Mode Selection

	Pin			
Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	O_0–O_7
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibition	High	High	V_{PP}	High impedance

Table 31 Recommended PROM Programmers and Socket Adapters

PROM Programmer			Socket Adapter		
Product Name	**Manufacturer**	**Model Name**	**Package**	**Model Name**	**Manufacturer**
HD4074729	DATA I/O Corp.	22B 29B	DP-64S DC-64S	HS470ESS11H	Hitachi
			FP-64B	HS470ESF01H	
			FP-64A	HS470ESH01H	
	AVAL DATA Corp.	PKW-1100 PKW-3100	DP-64S DC-64S	HS470ESS21H	
			FP-64B	HS470ESF01H	
			FP-64A	HS470ESH01H	
HD4074720	DATA I/O Corp.	22B 29B	DP-64S DC-64S	HS4720ESS01H	Hitachi
			FP-64B	HS4720ESF01H	
	AVAL DATA Corp.	PKW-1100 PKW-3100	DP-64S DC-64S	HS4720ESS01H	
			FP-64B	HS470ESF01H	

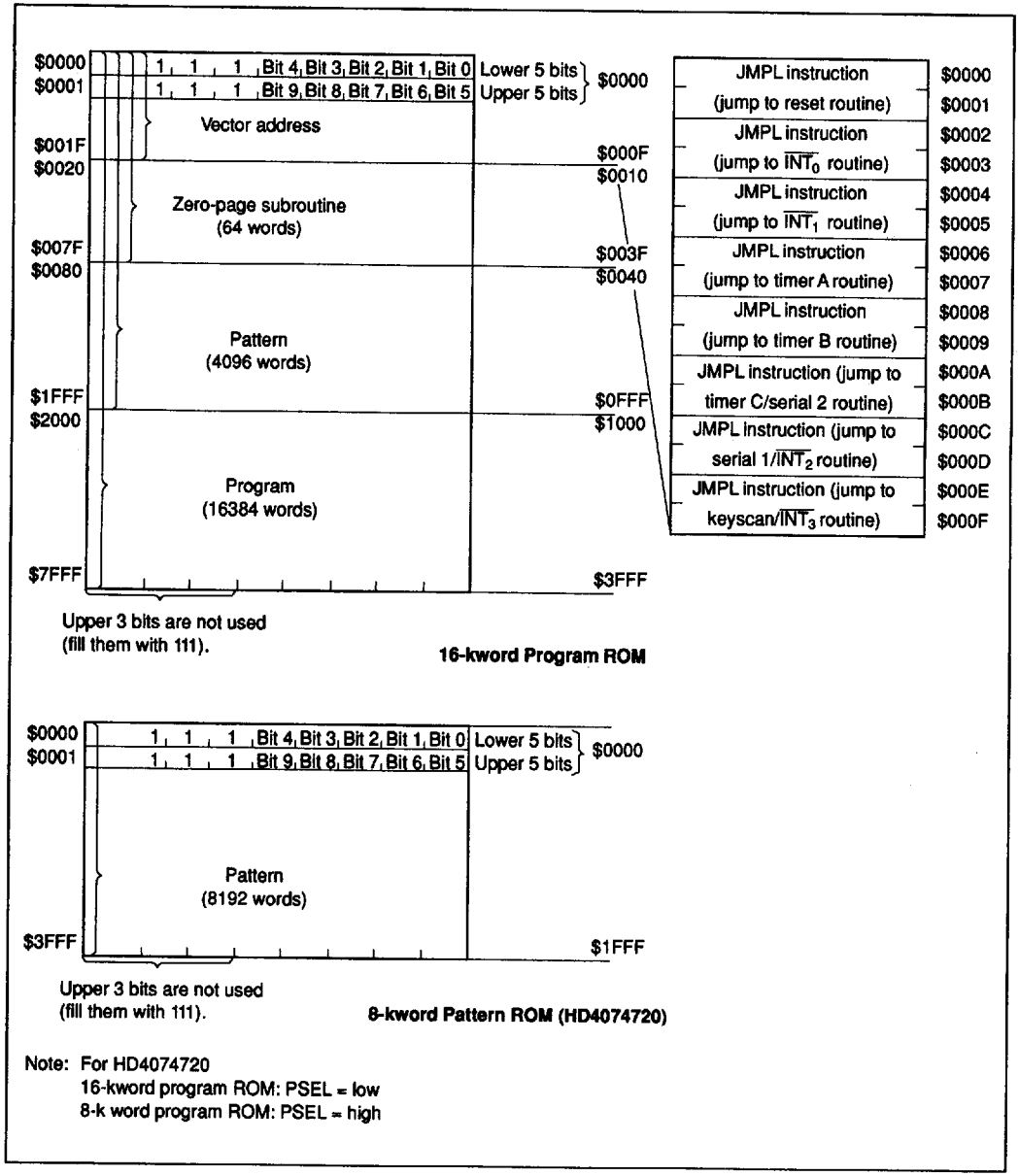


PSEL	PROM Select	Note	Compatible with
0	Program ROM (16 k)	Including pattern 1	27256
1	Pattern ROM (8 k)	Including patterns 2 and 3	27256

Notes: 1. The $R4_0/\overline{SCK_1}$ pin is assigned as the PSEL (pattern ROM select) input pin in PROM mode.

2. The program ROM (16 k) or pattern ROM (8 k) can be selected by the socket adapter switch, which sets PSEL at GND or V_{CC}.

Figure 50 Connections in PROM Mode



Note: For HD4074720
16-kword program ROM: PSEL = low
8-k word program ROM: PSEL = high

Figure 51 Map in PROM Mode

Addressing Modes

RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 52 and described below.

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory registers (MR), which consist of 16 digits from $040 to $04F, are accessed with the LAMR and XMRA instructions.

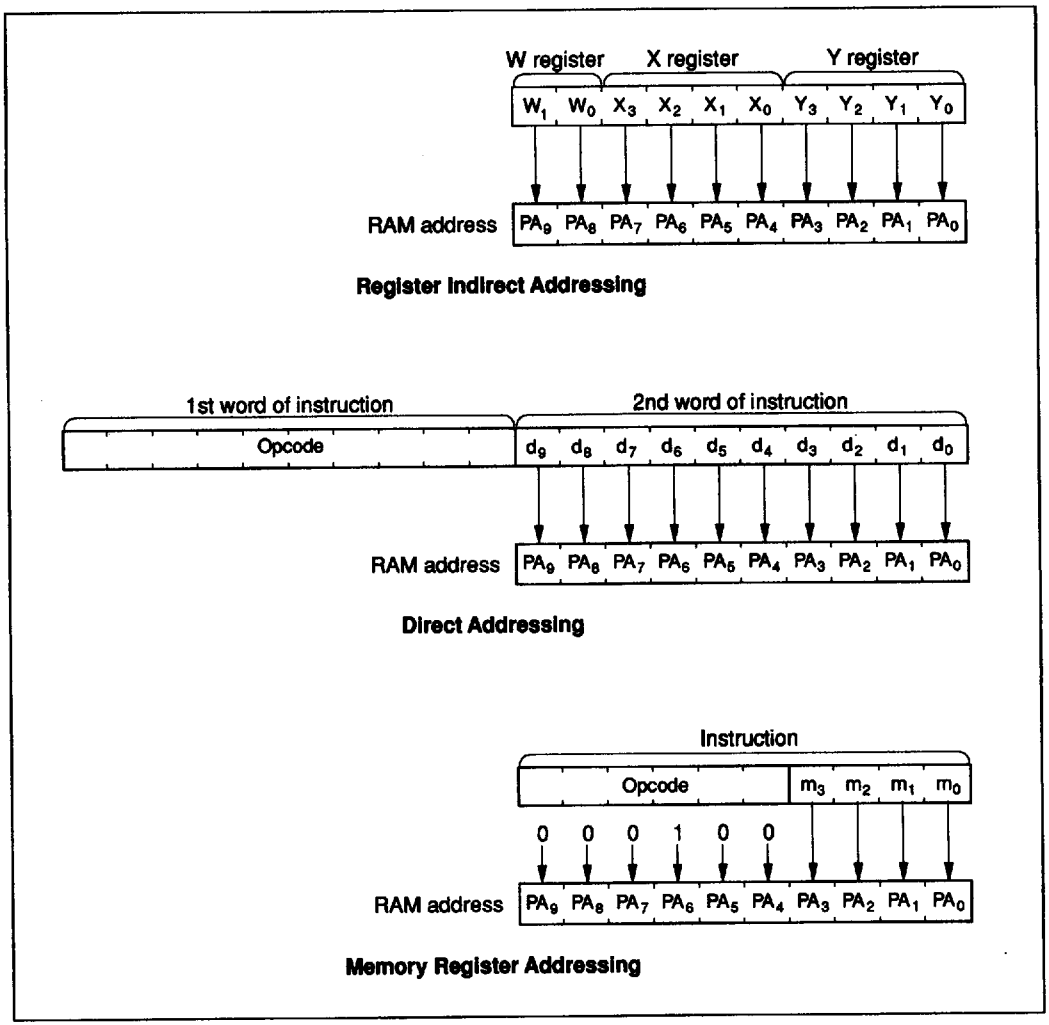


Figure 52 RAM Addressing Modes

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 53 and described below.

Direct Addressing Mode: A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13}–PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7–PC_0) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 55. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross macroassembler has an automatic paging feature for ROM pages.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at \$0000–\$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5–PC_0), and 0s are placed in the eight high-order bits (PC_{13}–PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figures 54-1 and 54-2. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

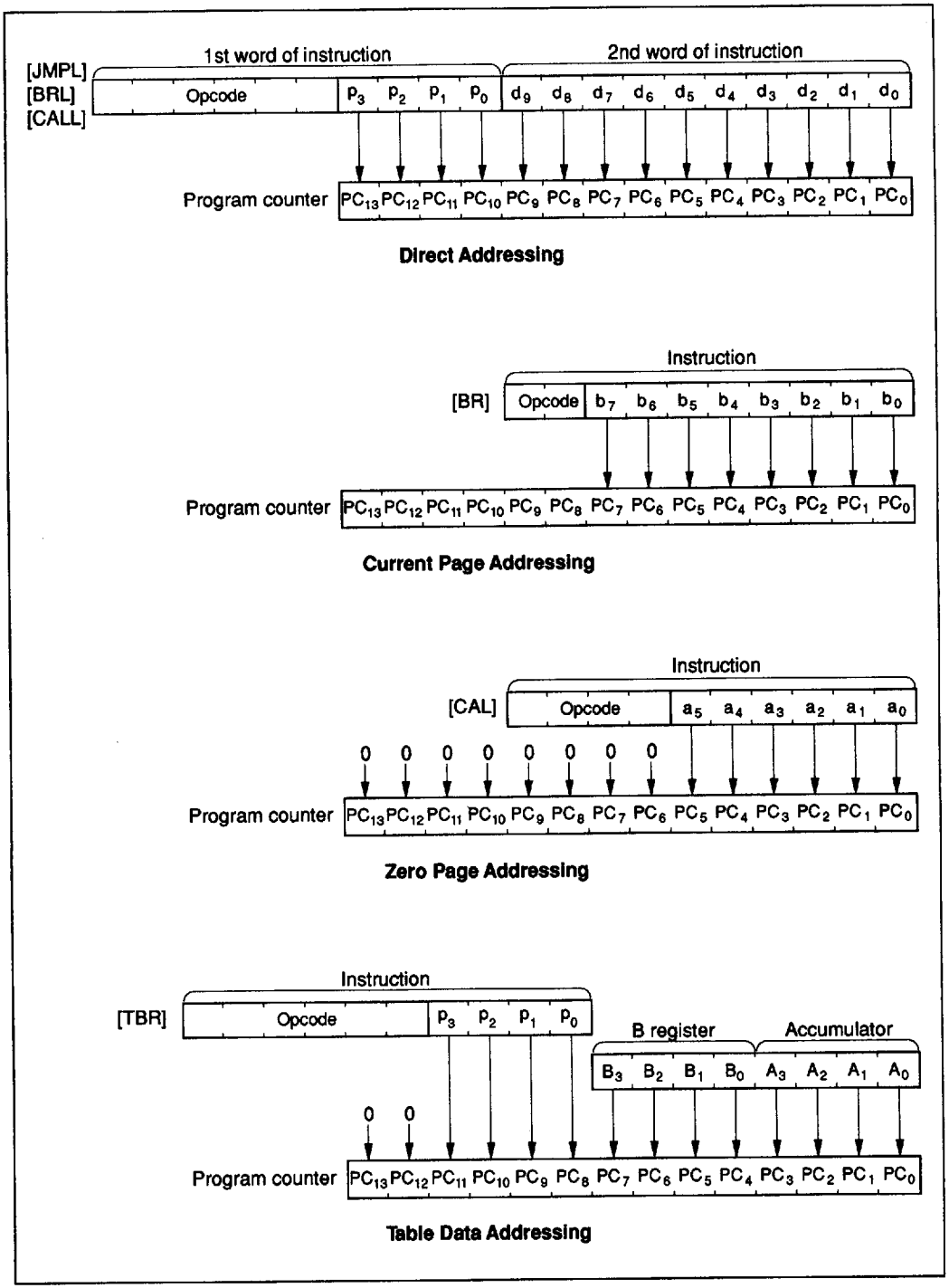


Figure 53 ROM Addressing Modes

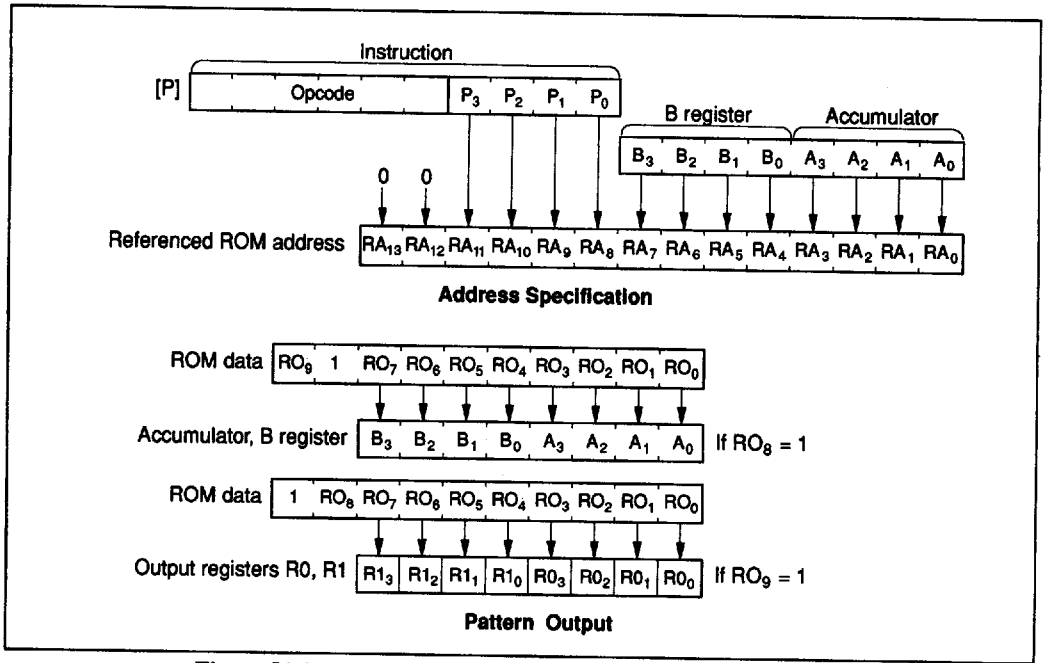


Figure 54-1 P Instruction (HD404728, HD404729, HD4074729)

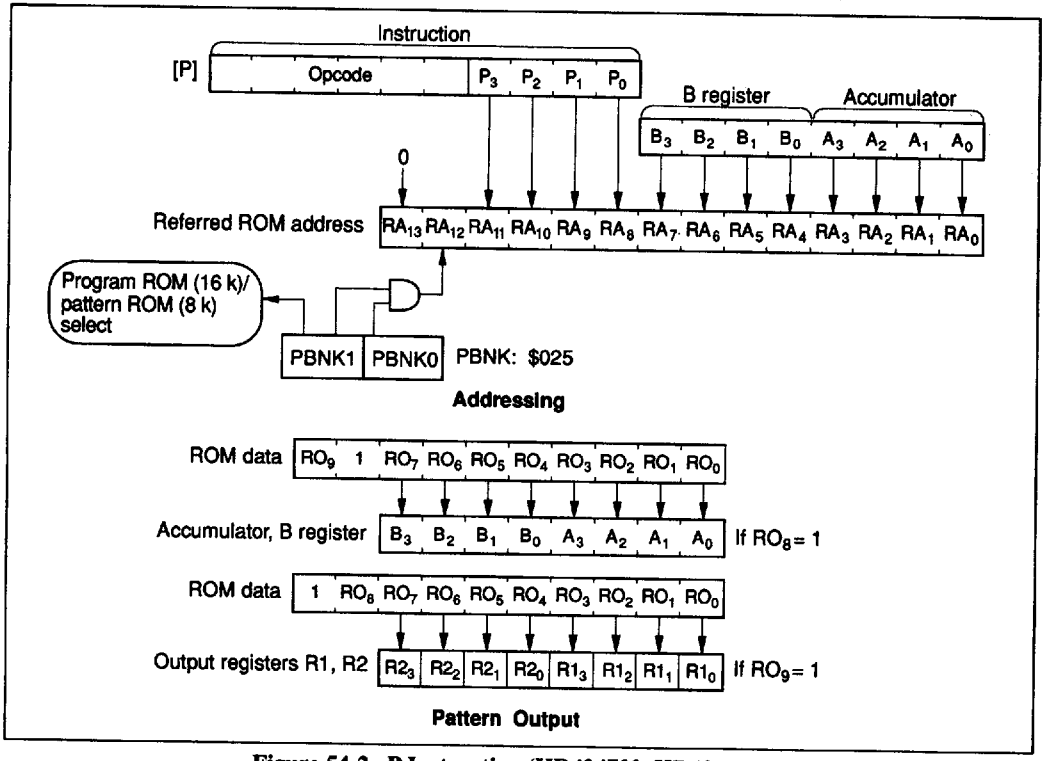


Figure 54-2 P Instruction (HD404720, HD4074720)

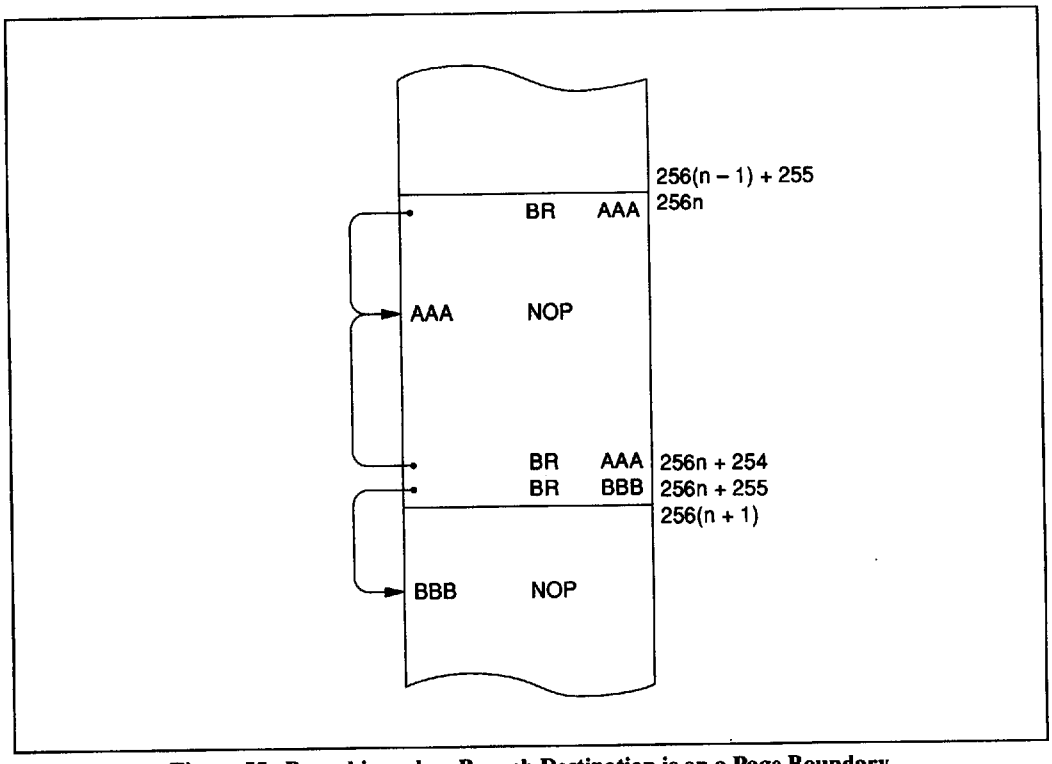


Figure 55 Branching when Branch Destination is on a Page Boundary

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	11
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	2
		V_{CC} – 45 to V_{CC} + 0.3	V	3
Total permissible input current	ΣI_o	50	mA	4
Total permissible output current	$-\Sigma I_o$	150	mA	5
Maximum input current	I_o	15	mA	6, 7
Maximum output current	$-I_o$	4	mA	8, 9
		30	mA	8, 10
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. All voltages are with respect to GND.
2. Standard pins.
3. High-voltage pins.
4. The total permissible input current is the total of input currents simultaneously flowing in from all I/O pins to GND.
5. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
6. The maximum input current is the maximum current flowing from any I/O pin to GND.
7. Applies to R4–R8.
8. The maximum output current is the maximum current flowing from V_{CC} to any I/O pin.
9. Applies to R4–R8.
10. Applies to D_0–D_{15} and R0–R3.
11. Applies to the HD4074729 and HD4074720.

Electrical Characteristics

DC Characteristics (HD404720, HD404728, HD404729: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C; HD4074720, HD4074729: V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition		Notes
Input high voltage	V_{IH}	RESET, $\overline{SCK_1}$, $\overline{SCK_2}$, $\overline{INT_0}$ to $\overline{INT_3}$	0.8V_{CC}	—	V_{CC} + 0.3	V			
		SI_1, SI_2	0.7V_{CC}	—	V_{CC} + 0.3	V			
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V	V_{CC} = 3.5 to 6.0 V	HD404720, HD404728, HD404729	
			V_{CC} – 0.5	—	V_{CC} + 0.3	V	V_{CC} = 3.5 to 5.5 V	HD4074720, HD4074729	
			V_{CC} – 0.3	—	V_{CC} + 0.3	V			
Input low voltage	V_{IL}	RESET, $\overline{SCK_1}$, $\overline{SCK_2}$, $\overline{INT_0}$ to $\overline{INT_3}$	–0.3	—	0.2V_{CC}	V			
		SI_1, SI_2	–0.3	—	0.3V_{CC}	V			
		OSC_1	–0.3	—	0.5	V	V_{CC} = 3.5 to 6.0 V	HD404720, HD404728, HD404729	
			–0.3	—	0.5	V	V_{CC} = 3.5 to 5.5 V	HD4074720, HD4074729	
			–0.3	—	0.3	V			
Output high voltage	V_{OH}	$\overline{SCK_1}$, $\overline{SCK_2}$, SO_1, SO_2, PWM, BUZZ	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA, V_{CC} = 3.5 to 6.0 V	HD404720, HD404728, HD404729	
			V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA, V_{CC} = 3.5 to 6.0 V		
			V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA, V_{CC} = 3.5 to 5.5 V	HD4074720, HD4074729	
			V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA, V_{CC} = 3.5 to 5.5 V		
			V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.3 mA		

DC Characteristics (HD404720, HD404728, HD404729: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C; HD4074720, HD4074729: V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition		Notes
Output low voltage	V_{OL}	$\overline{SCK_1}$, $\overline{SCK_2}$, SO_1, SO_2, PWM, BUZZ	—	—	0.4	V	I_{OL} = 1.6 mA, V_{CC} = 3.5 to 6.0 V	HD404720, HD404728, HD404729	
			—	—	0.4	V	I_{OL} = 1.6 mA, V_{CC} = 3.5 to 5.5 V	HD4074720, HD4074729	
			—	—	0.4	V	I_{OL} = 0.4 mA		
I/O leakage current	$\lvert I_{IL} \rvert$	RESET, $\overline{SCK_1}$, $\overline{SCK_2}$, $\overline{INT_0}$ to $\overline{INT_3}$ SI_1, SI_2, SO_1, SO_2, PWM, BUZZ, OSC_1	—	—	1	µA	V_{in} = 0.0 V to V_{CC}		1
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	11.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, 1/4 division ratio	HD404720, HD4074720	2, 5
			—	—	5.0	mA		HD404728	2, 5
			—	—	8.0	mA		HD404729, HD4074729	2, 5
			—	—	6.0	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz, 1/4 division ratio	HD404720, HD4074720	2, 5
			—	—	3.0	mA		HD404728	2, 5
			—	—	4.5	mA		HD404729, HD4074729	2, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, 1/4 division ratio		3, 5
			—	—	1.0	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz, 1/4 division ratio		3, 5
Current dissipation in subactive mode	I_{SUB}	V_{CC}	—	—	130	µA	V_{in} ($\overline{TEST}$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (RESET) = 0 to 0.3 V, V_{CC} = 3 V, 32.768 kHz crystal oscillator	HD404720	4
			—	—	200	µA		HD4074720	
			—	—	30	µA		HD404728	4
			—	—	80	µA		HD404729	4
			—	—	150	µA		HD4074729	

DC Characteristics (HD404720, HD404728, HD404729: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C; HD4074720, HD4074729: V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition		Notes
Current dissipation in watch mode	I_{WTC}	V_{CC}	—	—	15	µA	V_{in} ($\overline{TEST}$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (RESET) = 0 to 0.3 V, V_{CC} = 3 V, 32.768 kHz crystal oscillator	HD404720, HD404728, HD404729	4
			—	—	15	µA		HD4074720, HD4074729	
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	V_{in} ($\overline{TEST}$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (RESET) = 0 to 0.3 V, no 32.768 kHz crystal oscillator	HD404720, HD404728, HD404729	4
			—	—	10	µA	V_{in} ($\overline{TEST}$, $R9_0$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (RESET) = 0 to 0.3 V, no 32.768 kHz crystal oscillator	HD4074720, HD4074729	
Watch mode retaining voltage	V_{WTC}	V_{CC}	3.5	—	6.0	V	V_{CC} = 3.5 to 6.0 V	HD404720, HD404728, HD404729	
			3.0	—	6.0	V			
			3.5	—	5.5	V	V_{CC} = 3.5 to 5.5 V	HD4074720, HD4074729	
			3.0	—	5.5	V			
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V	No 32.768 kHz crystal oscillator		

Notes: 1. Excluding output buffer current (HD4074720, HD4074729).
Excluding output buffer current and pull-up MOS current (HD404720, HD404728, HD404729).

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.

Test condition	MCU	Reset
	Pins	• RESET, $\overline{TEST}$ at V_{CC} • R4–R9 at V_{CC} • D_0–D_{15}, R0–R3, RA at V_{disp}

3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is in operation.

Test condition	MCU	• I/O same as at reset • Serial interface halted • Standby mode
	Pins	• RESET at GND • $\overline{TEST}$ at V_{CC} • R4–R9 at V_{CC} • D_0–D_{15}, R0–R3, RA at V_{disp}

4. Excluding pull-down MOS current flowing to V_{disp}.

5. Power dissipation, while the MCU is operating or in standby mode, is in proportion to f_{OSC}. The value of the dissipation current when f_{OSC} = X MHz is given by the following equation:

Maximum value (f_{OSC} = X MHz) = X/4 × max value (f_{OSC} = 4 MHz)

Input/Output Characteristics for Standard Pins (HD404720, HD404728, HD404729: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C; HD4074720, HD4074729: V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition		Notes
Input high voltage	V_{IH}	R4 to R9	$0.7V_{CC}$	—	V_{CC} + 0.3	V			
Input low voltage	V_{IL}	R4 to R9	–0.3	—	$0.3V_{CC}$	V			
Output high voltage	V_{OH}	R4 to R8	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA, V_{CC} = 3.5 to 6.0 V	HD404720, HD404728, HD404729	
			V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA, V_{CC} = 3.5 to 5.5 V	HD4074720, HD4074729	
			V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA, V_{CC} = 3.5 to 6.0 V	HD404720, HD404728, HD404729	
			V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA, V_{CC} = 3.5 to 5.5 V	HD4074720, HD4074729	
			V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.3 mA		
Output low voltage	V_{OL}	R4 to R8	—	—	0.4	V	I_{OL} = 1.6 mA, V_{CC} = 3.5 to 6.0 V	HD404720, HD404728, HD404729	
			—	—	0.4	V	I_{OL} = 1.6 mA, V_{CC} = 3.5 to 5.5 V	HD4074720, HD4074729	
			—	—	0.4	V	I_{OL} = 0.4 mA		
Input/ output leakage current	$\lvert I_{IL} \rvert$	R4 to R9	—	—	1	µA	V_{in} = 0.0 V to V_{CC}	HD404720, HD404728, HD404729	1
		R4 to R8, $R9_1$ to $R9_3$	—	—	1	µA		HD4074720, HD4074729	2
		$R9_0$	—	—	30	µA		HD4074720	
			—	—	20	µA		HD4074729	
Pull-up MOS current	$-I_{PU}$	R4 to R9	30	70	150	µA	V_{CC} = 5 V, V_{in} = 0 V	HD404720, HD404728, HD404729	3
			10	20	50	µA	V_{CC} = 3 V, V_{in} = 0 V		

Notes: 1. Excluding pull-up MOS current and output buffer current.
2. Excluding output buffer current.
3. Applies to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High-Voltage Pins (HD404720, HD404728, HD404729: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C; HD4074720, HD4074729: V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition		Notes
Input high voltage	V_{IH}	D_0 to D_{15}, R0 to R3, RA	0.7V_{CC}	—	V_{CC} + 0.3	V			
Input low voltage	V_{IL}	D_0 to D_{15}, R0 to R3, RA	V_{CC} – 40	—	0.3V_{CC}	V			
Output high voltage	V_{OH}	D_0 to D_{15}, R0 to R3	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, V_{CC} = 5.0 V ±20%	HD404720, HD404728, HD404729	
			V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, V_{CC} = 4.0 V to 5.5 V	HD4074720, HD4074729	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 10 mA, V_{CC} = 5.0 V ±20%	HD404720, HD404728, HD404729	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 10 mA, V_{CC} = 4.0 V to 5.5 V	HD4074720, HD4074729	
			V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 4 mA		
Output low voltage	V_{OL}	D_0 to D_{15}, R0 to R3	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	HD404720, HD404728, HD404729	1
			—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V		2
			—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	HD4074720, HD4074729	
Input/ output leakage current	$\lvert I_{IL} \rvert$	D_0 to D_{15}, R0 to R3, RA	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}		3
Pull-down MOS current	I_{PD}	D_0 to D_{15}, R0 to R3, RA	200	400	800	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	HD404720, HD404728, HD404729	1

Notes: 1. Applies to I/O pins selected as with pull-down MOS by mask option.
2. Applies to I/O pins selected as without pull-down MOS (PMOS open drain) by mask option.
3. Excluding pull-down MOS current and output buffer current. (HD404720, HD404728, HD404729)
4. Excluding output buffer current. (HD4074720, HD4074729)

AC Characteristics (HD404720, HD404728, HD404729: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C; HD4074720, HD4074729: V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition		Notes
Oscillation frequency (1/4 division)	f_{OSC}	OSC_1, OSC_2	1.6	4	4.5	MHz	V_{CC} = 3.5 to 6.0 V	HD404720	
			0.4	4	4.5	MHz		HD404728, HD404729	7
			1.6	4	4.5	MHz			
			1.6	4	4.5	MHz	V_{CC} = 3.5 to 5.5 V	HD4074720	
			0.4	4	4.5	MHz		HD4074729	7
			1.6	4	4.5	MHz			
			1.6	2	2.25	MHz		HD404720, HD4074720	
			0.4	2	2.25	MHz		HD404728, HD404729, HD4074729	7
			1.6	2	2.25	MHz			
Oscillation frequency (1/8 division)	f_{CL}	CL_1, CL_2	—	32.768	—	kHz			
Instruction cycle time	t_{cyc}		0.89	1	2.5	µs	V_{CC} = 3.5 to 6.0 V	HD404720	
			0.89	1	10	µs		HD404728, HD404729	7
			0.89	1	2.5	µs			
			0.89	1	2.5	µs	V_{CC} = 3.5 to 5.5 V	HD4074720	
			0.89	1	10	µs		HD4074729	7
			0.89	1	2.5	µs			
			1.78	2	2.5	µs		HD404720, HD4074720	
			1.78	2	10	µs		HD404728, HD404729, HD4074729	7
			1.78	2	2.5	µs			
Instruction cycle time	t_{subcyc}		—	244.14	—	µs			
Oscillation stabilization time (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms	V_{CC} = 3.5 to 6.0 V	HD404720, HD404728, HD404729	1
			—	—	40	ms	V_{CC} = 3.5 to 5.5 V	HD4074720, HD4074729	1
			—	—	60	ms			1
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	20	ms	V_{CC} = 3.5 to 6.0 V	HD404720, HD404728, HD404729	1
			—	—	20	ms	V_{CC} = 3.5 to 5.5 V	HD4074720, HD4074729	1
			—	—	60	ms			1

AC Characteristics (HD404720, HD404728, HD404729: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C; HD4074720, HD4074729: V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition		Notes
Oscillation stabilization time	t_{RC}	CL_1, CL_2	—	—	2	s			2
External clock high width	t_{CPH}	OSC_1	92	—	—	ns	V_{CC} = 3.5 to 6.0 V	HD404720, HD404728, HD404729	3
			92	—	—	ns	V_{CC} = 3.5 to 5.5 V	HD4074720, HD4074729	3
			203	—	—	ns			3
External clock low width	t_{CPL}	OSC_1	92	—	—	ns	V_{CC} = 3.5 to 6.0 V	HD404720, HD404728, HD404729	3
			92	—	—	ns	V_{CC} = 3.5 to 5.5 V	HD4074720, HD4074729	3
			203	—	—	ns			3
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns	V_{CC} = 3.5 to 6.0 V	HD404720, HD404728, HD404729	3
			—	—	20	ns	V_{CC} = 3.5 to 5.5 V	HD4074720, HD4074729	3
			—	—	20	ns			3
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns	V_{CC} = 3.5 to 6.0 V	HD404720, HD404728, HD404729	3
			—	—	20	ns	V_{CC} = 3.5 to 5.5 V	HD4074720, HD4074729	3
			—	—	20	ns			3
$\overline{INT_0}$ high width	t_{IH}	$\overline{INT_0}$	2	—	—	t_{cyc} t_{subcyc}			4, 6
$\overline{INT_0}$ low width	t_{IL}	$\overline{INT_0}$	2	—	—	t_{cyc} t_{subcyc}			4, 6
$\overline{INT_1}$ high width	t_{IH}	$\overline{INT_0}$– $\overline{INT_3}$	2	—	—	t_{cyc}			4
$\overline{INT_1}$ low width	t_{IL}	$\overline{INT_0}$– $\overline{INT_3}$	2	—	—	t_{cyc}			4
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}			5

AC Characteristics (HD404720, HD404728, HD404729: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, HD4074720, HD4074729: V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition		Notes
Input capacitance	C_{in}	All pins	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	HD404720, HD404728, HD404729	
		All pins except $R9_0$	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	HD4074720, HD4074729	
		$R9_0$	—	—	270	pF	f = 1 MHz, V_{in} = 0 V	HD4074720	
			—	—	180	pF		HD4074729	
RESET fall time	t_{RSTf}	RESET	—	—	20	ms			5

Notes: 1. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 3.0 V (3.5 V if V_{CC} = 3.5 to 6.0 V: HD404720/HD404728/HD404729; V_{CC} = 3.5 to 5.5 V: HD4074720/HD4074729) at power-on or after RESET input goes high after stop mode is cancelled (figure 56). At power-on and when stop mode is cancelled, RESET must remain high for at least t_{RC} to ensure the oscillation stabilization time. If using a crystal oscillator, contact the manufacturer to determine what oscillation stabilization time is required, since it depends on the circuit constants and stray capacitances.

2. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 3.0 V at power-on (figure 57). The oscillation stabilization time (t_{RC}) must be ensured. If using a crystal oscillator, contact the manufacturer to determine what oscillation stabilization time is required, since it depends on the circuit constants and stray capacitances.
3. Refer to figure 58.
4. Refer to figure 59.
5. Refer to figure 60.
6. The t_{subcyc} unit applies when the MCU is in watch or subactive mode.
   t_{subcyc} = 244.14 µs (32.768-kHz crystal)

Serial Interface Timing Characteristics (HD404720, HD404728, HD404729: V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C; HD4074720, HD4074729: V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20°C to +75°C, unless otherwise specified)

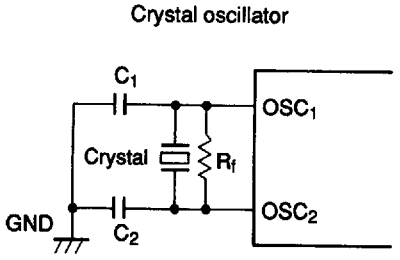
Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Output transmit clock cycle time	t_{Scyc}	$\overline{SCK_1}$, $\overline{SCK_2}$	1	—	—	t_{cyc}	Load shown in figure 62	1
Output transmit clock high width	t_{SCKH}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}	Load shown in figure 62	1
Output transmit clock low width	t_{SCKL}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}	Load shown in figure 62	1
Output transmit clock rise time	t_{SCKr}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	80	ns	Load shown in figure 62	1
Output transmit clock fall time	t_{SCKf}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	80	ns	Load shown in figure 62	1
Input transmit clock cycle time	t_{Scyc}	$\overline{SCK_1}$, $\overline{SCK_2}$	2	—	—	t_{cyc}		1
Input transmit clock high width	t_{SCKH}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.8	—	—	t_{Scyc}		1
Input transmit clock low width	t_{SCKL}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.8	—	—	t_{Scyc}		1
Input transmit clock rise time	t_{SCKr}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	80	ns		1
Input transmit clock fall time	t_{SCKf}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO_1, SO_2	—	—	600	ns	Load shown in figure 62	1
Serial input data setup time	t_{SSI}	SI_1, SI_2	200	—	—	ns		1
Serial input data hold time	t_{HSI}	SI_1, SI_2	400	—	—	ns		1

Note: 1. Refer to figure 61.

Serial Interface Timing Characteristics (HD404720, HD404728, HD404729: V_{CC} = 3.5 to 6.0 V, HD4074720, HD4074729: V_{CC} = 3.5 to 5.5 V)

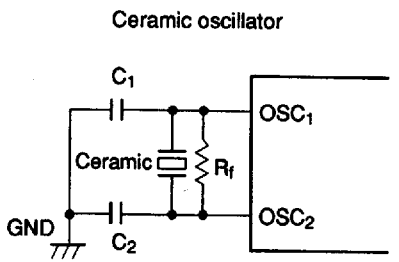
Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Output transmit clock cycle time	t_{Scyc}	$\overline{SCK_1}$, $\overline{SCK_2}$	1	—	—	t_{cyc}	Load shown in figure 62	1
Output transmit clock high width	t_{SCKH}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}	Load shown in figure 62	1
Output transmit clock low width	t_{SCKL}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}	Load shown in figure 62	1
Output transmit clock rise time	t_{SCKr}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	40	ns	Load shown in figure 62	1
Output transmit clock fall time	t_{SCKf}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	40	ns	Load shown in figure 62	1
Input transmit clock cycle time	t_{Scyc}	$\overline{SCK_1}$, $\overline{SCK_2}$	2	—	—	t_{cyc}		1
Input transmit clock high width	t_{SCKH}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.8	—	—	t_{Scyc}		1
Input transmit clock low width	t_{SCKL}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.8	—	—	t_{Scyc}		1
Input transmit clock rise time	t_{SCKr}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	40	ns		1
Input transmit clock fall time	t_{SCKf}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	40	ns		1
Serial output data delay time	t_{DSO}	SO_1, SO_2	—	—	300	ns	Load shown in figure 62	1
Serial input data setup time	t_{SSI}	SI_1, SI_2	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI_1, SI_2	200	—	—	ns		1

Note: 1. Refer to figure 61.



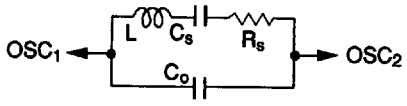
Crystal: Equivalent to the circuit below

R_f: 1 MΩ ± 20%
C_1: 10 pF ± 20%
C_2: 10 pF ± 20%



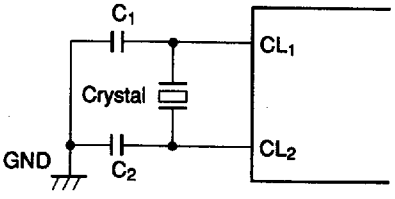
Ceramic oscillator: CSA4.00MG (Murata)

R_f: 1 MΩ ± 20%
C_1: 30 pF ± 20%
C_2: 30 pF ± 20%



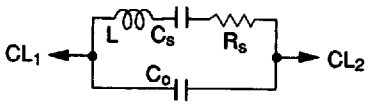
C_o = 7 pF, max.
R_s = 100 Ω, max.
f = 1.6 to 4.5 MHz

Figure 56 Oscillation Circuits (1)



Crystal: MX38T (Nihon Denpa Kogyo)
Equivalent to the circuit on the right

C_1: 15 pF ± 5%
C_2: 15 pF ± 5%



C_o = 1.5 pF, typ.
R_s = 14 kΩ, typ.
f = 32.768 kHz

Figure 57 Oscillation Circuits (2)

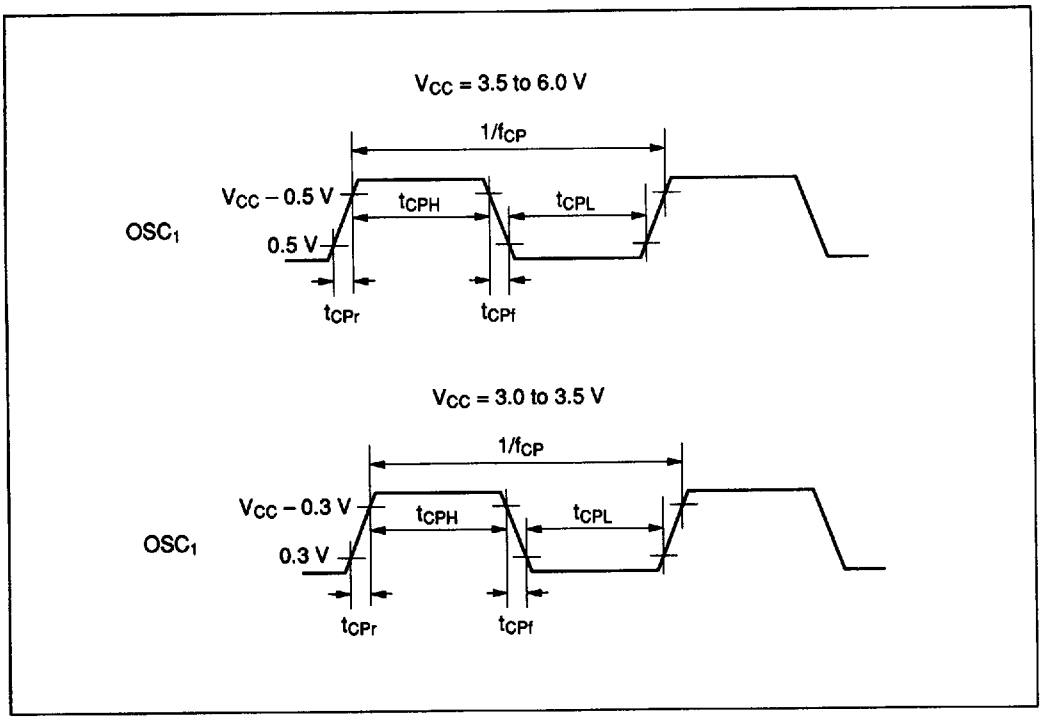


Figure 58 Oscillator Timing

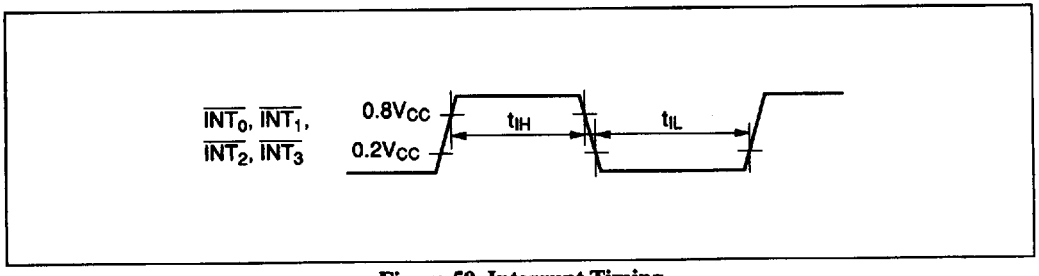


Figure 59 Interrupt Timing

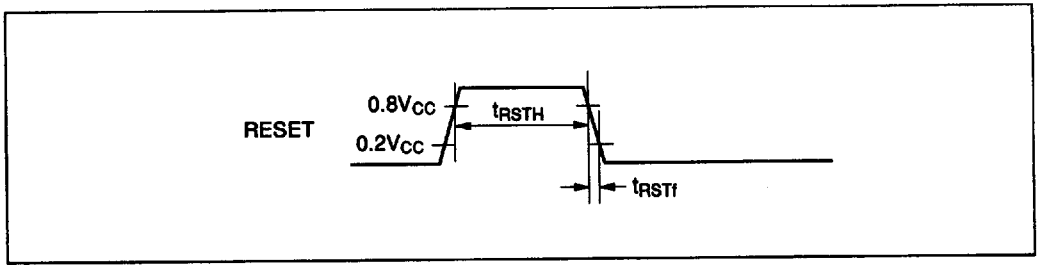
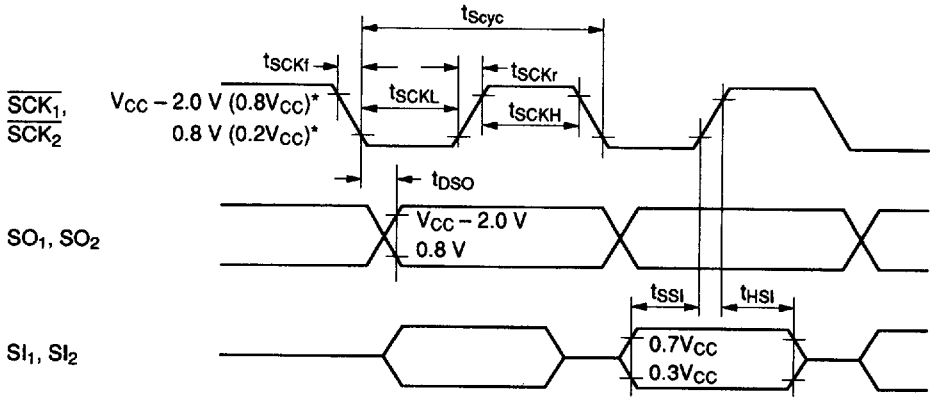


Figure 60 Reset Timing



* V_{CC} – 2.0 V and 0.8 V are valid when the transmit clock is output.
0.8V_{CC} and 0.2V_{CC} are valid when the transmit clock is input.
t_{DSO}, t_{SSI}, and t_{HSI} are determined by the voltage at transmit clock input.

Figure 61 Serial Interface Timing

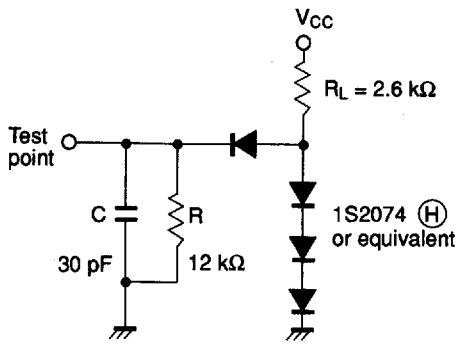


Figure 62 Timing Load Circuit

HD404728, HD404729 Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number	

1. ROM Size

☐ HD404728	8-kword
☐ HD404729	16-kword

2. Optional Functions

*☐ With 32-kHz CPU operation, with time-base for clock
*☐ Without 32-kHz CPU operation, with time-base for clock
☐ Without 32-kHz CPU operation, without time-base

Note: * Options marked with an asterisk require a subsystem crystal oscillator (CL1, CL2).

3. I/O Options (shaded options are not available)

B: With pull-up MOS C: Without pull-up MOS
D: Without pull-down MOS E: With pull-down MOS

Pin name		I/O		I/O option			
				B	C	D	E
D0		High-voltage pins	I/O				
D1			I/O				
D2			I/O				
D3			I/O				
D4			I/O				
D5			I/O				
D6			I/O				
D7			I/O				
D8			I/O				
D9			I/O				
D10			I/O				
D11			I/O				
D12			I/O				
D13			I/O				
D14			I/O				
D15			I/O				
R0	R00		I/O				
	R01		I/O				
	R02		I/O				
	R03		I/O				
R1	R10		I/O				
	R11		I/O				
	R12		I/O				
	R13		I/O				
R2	R20		I/O				
	R21		I/O				
	R22		I/O				
	R23		I/O				

Pin name		I/O		I/O option			
				B	C	D	E
R3	R30	High-voltage pins	I/O				
	R31		I/O				
	R32		I/O				
	R33		I/O				
R4	R40	Standard pins	I/O				
	R41		I/O				
	R42		I/O				
	R43		I/O				
R5	R50		I/O				
	R51		I/O				
	R52		I/O				
	R53		I/O				
R6	R60		I/O				
	R61		I/O				
	R62		I/O				
	R63		I/O				
R7	R70		I/O				
	R71		I/O				
	R72		I/O				
	R73		I/O				
R8	R80		I/O				
	R81		I/O				
R9	R90		I/O				
	R91		I/O				
	R92		I/O				
	R93		I/O				
RA	RA0	High-voltage pins	I/O				
	RA1		I/O	Checklist 4			

4. RA1/Vdisp

☐ RA1: Without pull-down MOS (D)
☐ Vdisp

Note: If even one high-voltage pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

5. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

6. OSC1 and OSC2 Oscillator

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

7. Stop Mode

☐ Used
☐ Not used

8. Package

☐ DP-64S
☐ FP-64A
☐ FP-64B

HD404720 Option List

Please check off the appropriate applications and enter the necessary information.

Date of order		
Customer		
Department		
Name		
ROM code name	16-k program ROM	
	8-k pattern ROM	
LSI number (Hitachi's entry)		

1. Optional Functions

*☐ With 32-kHz CPU operation, with time-base for clock
*☐ Without 32-kHz CPU operation, with time-base for clock
☐ Without 32-kHz CPU operation, without time-base

Note: * Options marked with an asterisk require a subsystem crystal oscillator (CL1, CL2).

2. I/O Options (shaded options are not available)
   B: With pull-up MOS
   C: Without pull-up MOS
   D: Without pull-down MOS
   E: With pull-down MOS

Pin name		I/O		I/O option			
				B	C	D	E
D0		High-voltage pins	I/O				
D1			I/O				
D2			I/O				
D3			I/O				
D4			I/O				
D5			I/O				
D6			I/O				
D7			I/O				
D8			I/O				
D9			I/O				
D10			I/O				
D11			I/O				
D12			I/O				
D13			I/O				
D14			I/O				
D15			I/O				
R0	R00		I/O				
	R01		I/O				
	R02		I/O				
	R03		I/O				
R1	R10		I/O				
	R11		I/O				
	R12		I/O				
	R13		I/O				
R2	R20		I/O				
	R21		I/O				
	R22		I/O				
	R23		I/O				

Pin name		I/O		I/O option			
				B	C	D	E
R3	R30	High-voltage pins	I/O				
	R31		I/O				
	R32		I/O				
	R33		I/O				
R4	R40	Standard pins	I/O				
	R41		I/O				
	R42		I/O				
	R43		I/O				
R5	R50		I/O				
	R51		I/O				
	R52		I/O				
	R53		I/O				
R6	R60		I/O				
	R61		I/O				
	R62		I/O				
	R63		I/O				
R7	R70		I/O				
	R71		I/O				
	R72		I/O				
	R73		I/O				
R8	R80		I/O				
	R81		I/O				
R9	R90		I				
	R91		I				
	R92		I				
	R93		I				
RA	RA0	High-voltage pins	I				
	RA1		I	Checklist 3			

3. RA1/Vdisp

☐ RA1: Without pull-down MOS (D)
☐ Vdisp

Note: If even one high-voltage pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

4. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

5. OSC1 and OSC2 Oscillator

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

6. Stop Mode

☐ Used
☐ Not used

7. Package

☐ DP-64S
☐ FP-64B