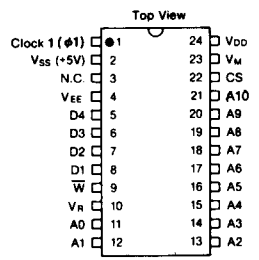
8192 Bit Electrically Alterable Read Only Memory

FEATURES

- 2048 word x 4 bit organization
- 11 bit binary addressing
- ±5, −14, −24V power supplies
- Block erasable
- 1 year unpowered data storage
- TTL compatible with pull up resistors on inputs
- Tri-state outputs
- Read time: 1.6μs
- Write time: 10ms, erase time: 100ms
- Chip select

PIN CONFIGURATION

24 LEAD DUAL IN LINE



DESCRIPTION

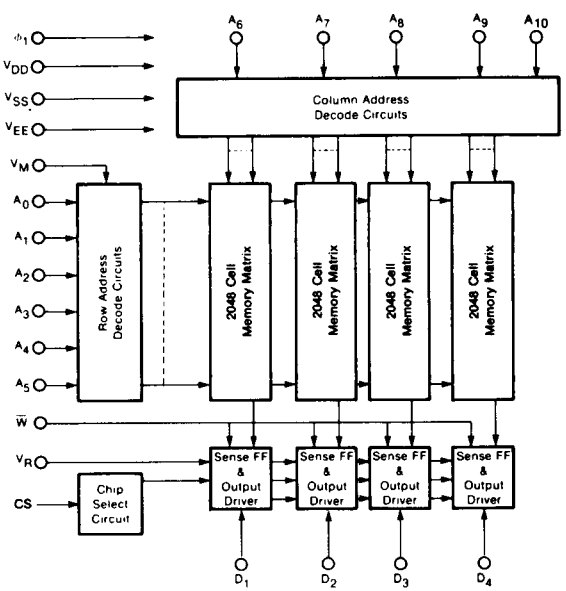
The ER2810 IR and ER2810 HR are fully decoded 2048 x 4-bit electrically erasable and reprogrammable ROMs utilizing second-generation MNOS epitaxial processing technology.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 8192 MNOS memory transistors. When the writing voltage is removed, the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

The ER2810 IR and ER2810 HR are screened to Mil Std. 883B/ method 5004.1/level B, pre-cap visual inspection, environmental testing, burn-in and external visual. They are available in 24 lead ceramic dual in line packages.

Stored data may be accessed a minimum of 2×10^{10} times without refresh and is non-volatile in the unpowered state in excess of one year. Data is erased by applying a V_{SS} −28V pulse to the erase substrate of the device. Data may be reprogrammed, without degradation of the retention time, up to 10^5 times, beyond which a gradual, logarithmic fall off is seen. All outputs are at logic high when the device is in the erased state.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs relative to V_{SS} ..... +0.3V to −30V
Storage temperature ..... −65° C to +150° C
Soldering temperature of leads (10 seconds) ..... +300° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

RECOMMENDED OPERATING CONDITIONS T_A = −40° C to +85° C for ER2810IR
T_A = −55° C to +95° C for ER2810HR

Symbol	Parameter	Erase Mode			Write Mode			Read Mode			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{DD}	Supply Voltage	4.75	V_{SS}	V_{SS}+0.3	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{SS}	Substrate supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_M	Memory voltage	—	V_{SS}	—	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-10.5	V_{SS}-10	V_{SS}-9.5	V
V_R	Reference voltage	—	V_{SS}	—	—	V_{SS}	—	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{EEH}	Erase substrate input high	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V
V_{EEL}	Erase substrate input low	V_{SS}-29	V_{SS}-28	V_{SS}-27	Not Applicable			Not Applicable			V
V_{WH}	Write control input high	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{WL}	Write control input low	V_{SS}-29	—	V_{SS}-4.4	V_{SS}-29	—	V_{SS}-4.4	Not Applicable			V
$V\phi_H$	ϕ_1 input high voltage	—	V_{SS}	—	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V
$V\phi_L$	ϕ_1 input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
V_{IH}	Address and CS input high	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{IL}	Address and CS input low	Don't Care			V_{DD}	—	V_{SS}-4.4	V_{DD}	—	V_{SS}-4.4	V
V_{DH}	Data input high voltage	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	Not Applicable			V
V_{DL}	Data input low voltage	Don't Care			V_{DD}	—	V_{SS}-4.4	Not Applicable			V

STATIC ELECTRICAL CHARACTERISTICS T_A = −40° C to +85° C for ER2810IR
T_A = −55° C to +95° C for ER2810HR
(NO EXTERNAL LOADS EXCEPT AS NOTED)

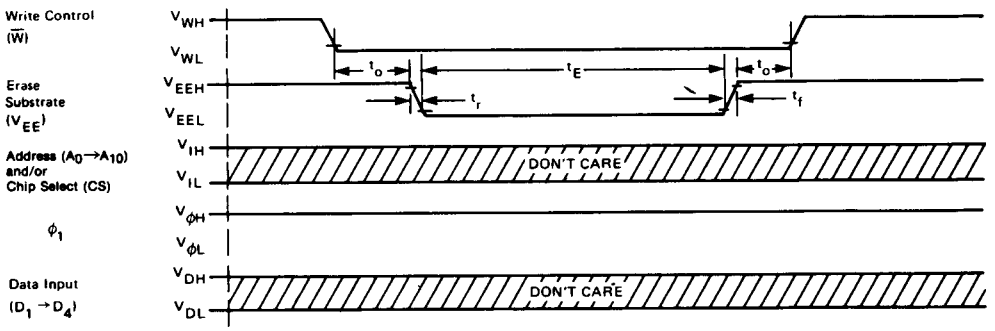
Symbol	Parameter	Conditions All Pins at V_{SS} Unless Noted	Min	Typ	Max	Unit
I_{IN}	Input leakage current (except pins 1, 2, 4, 5, 6, 7, 8, and 24) at V_{SS}-15V	$\phi 1 = V_{DD} = V_{SS}$-20	—	—	-2.0	μA
$I\phi_1$	ϕ_1 leakage current at V_{SS}-29V	$V_{DD} = V_{SS}$-29, $\overline{W} = V_{SS}$-25	—	—	-200	μA
I_O	Output leakage current at V_{SS}-15V	Chip deselected	—	—	-10.0	μA
I_{EEL}	Erase leakage current at V_{SS}-28V	$\overline{W} = V_{SS}$-25	—	—	-200	μA
I_{DD1}	V_{DD} supply current - read mode at V_{SS}-19V	Outputs open (See Figure 6)	—	16	20	mA
I_{DD2}	V_{DD} supply current - Write mode at V_{SS}-28V	Outputs open (See Figure 5)	—	30	40	mA
V_{OH}	Data output high voltage - TTL load	One Series 7400 TTL load with R_S = 1K, $V_{CC} = V_{SS}$ (See TTL Notes)	V_{SS} −1.5	—	—	V
V_{OL}	Data output low voltage - TTL load		—	—	V_{SS} −10	V
V_{OH}	Data Output high voltage - MOS		V_{SS}-1.5	—	—	V
V_{OL}	Data Output low voltage — MOS	C_L = 100pF	—	—	V_{SS} −14	V
T_S	Unpowered nonvolatile data storage	Typical write conditions	1	—	—	Years

CAPACITANCE AT $V_{IN} = V_{SS}$, ALL OTHER PINS GROUNDED (V_{SS}), f = 1MHz

Symbol	Parameter	Min	Typ	Max	Unit
C_I	Address and chip select input capacitance	—	5	7	pF
C_W	Write control input capacitance	—	10	20	pF
C_{ST}	Strobe input capacitance	—	10	15	pF
$C\phi_1$	ϕ_1 Input Capacitance	—	40	50	pF
C_{EE}	Erase substrate capacitance	—	600	700	pF
C_D	Data input/output capacitance	—	6	10	pF

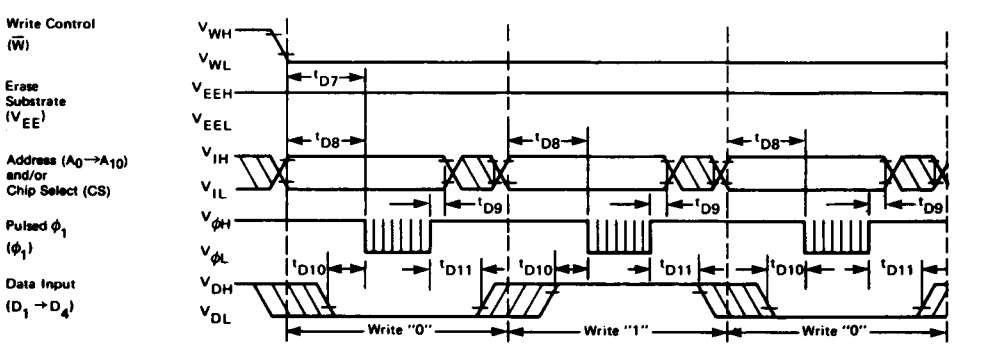
ERASE CYCLE CHARACTERISTICS $T_A = -40°C$ to $+85°C$ for ER2810IR
$T_A = -55°C$ to $+95°C$ for ER2810HR

Symbol	Parameter	Min	Typ	Max	Units
t_E	V_{EE} erase pulse width	100	—	1000	ms
t_R, t_F	V_{EE} rise time, V_{EE} fall time	0.01	—	1.0	ms
t_O	Write-erase overlap	10	—	—	μs



WRITE CYCLE CHARACTERISTICS $T_A = -40°C$ to $+85°C$ for ER2810IR
$T_A = -55°C$ to $+95°C$ for ER2810HR (See Note 3)

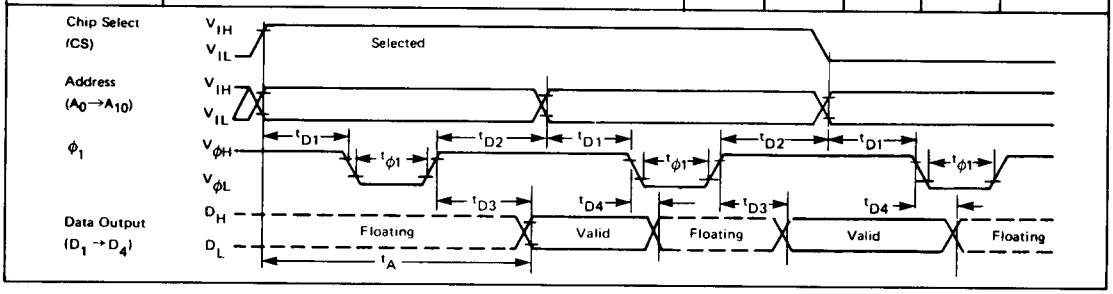
Symbol	Parameter	Min	Typ	Max	Units
$N\phi_W$	Number of ϕ_1 write pulses at 100 μs ±10%, 5 μs min. dead time between pulses)	100	200	300	Pulses
t_{D7}	Write control rise to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D8}	Address change and chip select fall to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D9}	Pulsed ϕ_1 fall to address and chip select change delay	0.0	—	—	μs
t_{D10}	Data input change to pulsed ϕ_1 rise delay	0.0	—	—	μs
t_{D11}	Pulsed ϕ_1 fall to data input change delay	0.0	—	—	μs
N_W	Number of times word may be rewritten	—	—	10^5	—



NOTES:
1. Due to the dynamic nature of the circuit a "ϕ_1 NOT" time in excess of 40 μsec may result in a floated output condition. Consequently data must be resampled with a 40 μsec time period following the fall of ϕ_1 to ensure its validity.
2. Several seconds may be required following a programming operation for the circuit to become operable in the read mode. If data is to be verified immediately following programming, a forward current of +1mA ± 10% may be forced into the erase substrate junction (Pin 4, V_{EE}), for a period not to exceed 10 milliseconds, to quickly dissipate charge trapped at internal circuit nodes.
3. Maximum power dissipation occurs during programming. When programming multichip systems where the application of programming voltages is required for several minutes, forced air cooling is recommended to reduce package temperature. Power is not reduced when chip is deselected.
4. All typical values are at +25°C and nominal voltages.
5. ϕ pulses are required after the fall of the chip select line to force the data outputs into a high impedance state.

READ CYCLE CHARACTERISTICS $T_A = -40°C$ to $+85°C$ for ER2810IR
$T_A = -55°C$ to $+95°C$ for ER2810HR

Symbol	Parameter (See Figures 1 through 4)	Min	Typ	Max	Units	
T_A	Access time	—	1.6	2.0	μs	
$t_{\phi 1}$	Pulse width (rise and fall times ≤50ns) (See Note 1)	800	—	5000	ns	
t_{D1}	Address and chip select change to ϕ_1 fall delay	400	—	—	ns	
t_{D2}	ϕ_1 Rise to address and chip select change delay	50	—	—	ns	See Note 1
t_{D3}	ϕ_1 Rise to data output valid delay (See Notes 1 and 2)	—	—	750	ns	See Note 1
t_{D4}	ϕ_1 Fall to floated output delay	—	—	300	ns	
N_{RA}	Number of read accesses/word between refresh	2×10^{10}	—	—	—	



PIN FUNCTIONS

Chip Select (CS)
Must be in the high state to enable the data output terminals or to write data into the device.

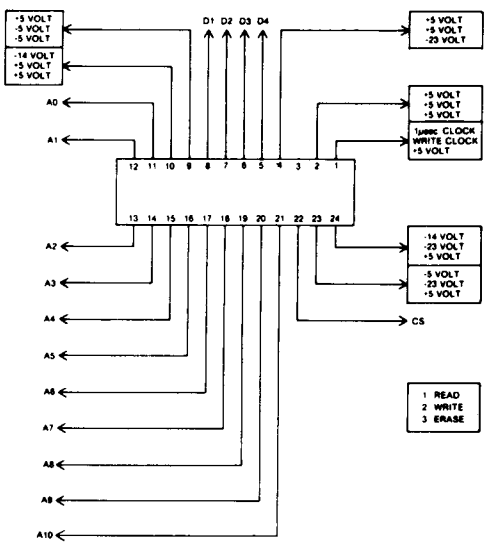
Data Input/Output (D1-D4)
D1 through D4 are bidirectional data terminals. Data are entered on these terminals during the write cycle and read out during the read cycle. When deselected, these terminals are in a floating condition.

Write Control ($\overline{W}$)
The write control terminal must be in the low state in order to write data into the device.

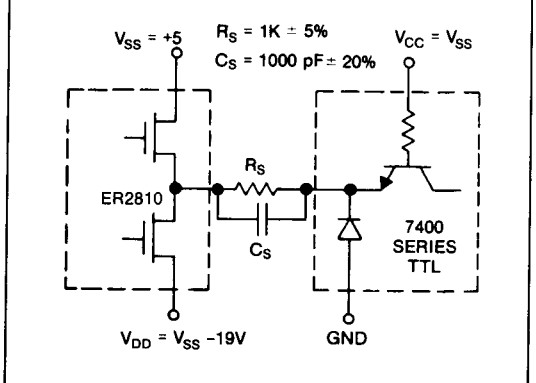
Phase One ($\phi 1$)
During the write and read operations, pulses must be applied to the $\phi 1$ terminal to fully shift the memory transistor threshold voltage to its most negative state. This is required for voltage bootstrapping in the row-selection circuitry. The $\phi 1$ input is high level and not TTL-compatible.

NOTE: All control, address and data inputs are TTL-compatible with pull-up resistors.

ER2810 OPERATION



TTL INTERFACE



MOS INTERFACE