National Semiconductor Corporation

PRELIMINARY

DM54ALS5245/DM74ALS5245 Octal TRI-STATE® Transceivers

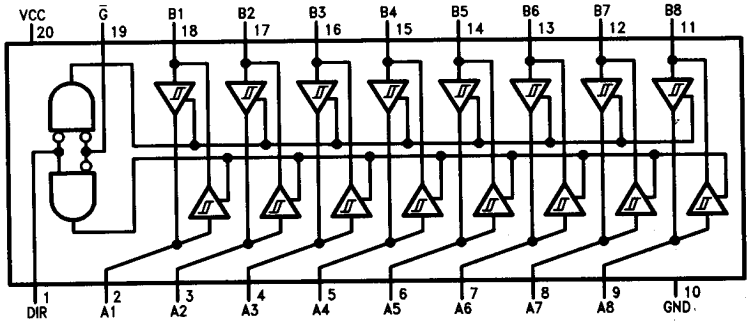
General Description

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The inputs include hystersis which provides improved noise rejection. Data is transmitted either from the A bus to the B bus or from the B bus to the A bus depending on the logic level of the direction control (DIR) input. The device can be disabled via the enable input ($\overline{G}$) which causes the outputs to enter the high impedance mode so the buses are effectively isolated.

Features

- Advanced oxide-isolated, ion implanted Schottky TTL process
- Switching specification guaranteed over the full temperature and V_{CC} range
- PNP inputs to reduce input loading
- Input Hystersis to improve noise margin

Connection Diagram



TL/F/9175–1

Order Number DM54ALS5245J, DM74ALS5245WM or DM74ALS5245N
See NS Package Number J20A, M20B or N20A

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	High Impedance

L = Low Logic Level, H = High Logic Level
X = Don't Care (Either Low or High Logic Level)

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free-Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS5245			DM74ALS5245			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature Range	−55		125	0		70	°C

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		DM54ALS5245			DM74ALS5245			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
H_{YS}	Hystersis ($V_{T+} - V_{T-}$)	V_{CC} = Min		0.2	0.4		0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = Min	I_{OH} = 3 mA	2.4	3.2		2.4	3.2		
			I_{OH} = Max	2			2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	I/O Ports, V_I = 5.5V			100			100	μA
			Control Inputs, V_I = 7V			100			100	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V (Note 1)				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 1)				−100			−100	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		30	48		30	45	mA
			Outputs Low		36	60		36	55	
			Outputs Disabled		38	63		38	58	

Note 1: For I/O ports, I_{IH} and I_{IL} parameters include the TRI-STATE output currents (I_{OZL} and I_{OZH}).

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS5245		DM74ALS5245		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, $R_1 = R_2 = 500\Omega$, C_L = 50 pF (Note 1)	A or B to B or A	3	15	3	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B to B or A	3	13	3	10	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$ to A or B	5	25	5	20	ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$ to A or B	5	25	5	20	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$ to A or B	2	12	2	10	ns
t_{PLZ}	Output DisableTime from Low Level Output		$\overline{G}$ to A or B	4	18	4	15	ns

Note 1: See Section 1 for test waveforms and output load.