# HCPL-4506/J456/0466
# HCNW4506

Intelligent Power Module and Gate Drive Interface Optocouplers

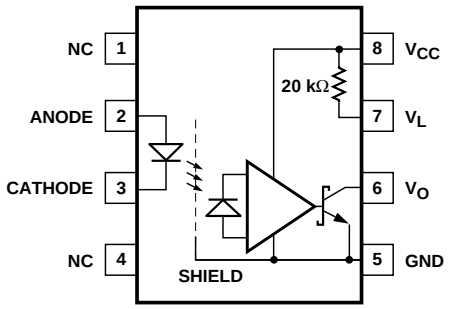
## Data Sheet

### Description

The HCPL-4506 and HCPL-0466 contain a GaAsP LED while the HCPL-J456 and the HCNW4506 contain an AlGaAs LED. The LED is optically coupled to an integrated high gain photo detector. Minimized propagation delay difference between devices makes these optocouplers excellent solutions for improving inverter efficiency through reduced switching dead time.

An on chip 20 kΩ output pull-up resistor can be enabled by shorting output pins 6 and 7, thus eliminating the need for an external pull-up resistor in common IPM applications. Specifications and performance plots are given for typical IPM applications.

### Functional Diagram




### Truth Table

| LED | $V_O$ |
|---|---|
| ON | L |
| OFF | H |

The connection of a 0.1 µF bypass capacitor between pins 5 and 8 is recommended.

### Features

- **Performance specified for bommon IPM applications over industrial temperature range: -40°C to 100°C**
- **Fast maximum propagation delays**
  **$t_{PHL}$ = 480 ns**
  **$t_{PLH}$ = 550 ns**
- **Minimized Pulse Width Distortion**
  **PWD = 450 ns**
- **15 kV / µs minimum common mode transient immunity at $V_{CM}$ = 1500 V**
- **CTR > 44% at $I_F$ = 10 mA**
- **Safety approval:**
  **UL Recognized**
  -3750 V rms / 1 min. for HCPL-4506 / 0466 / J456
  -5000 V rms / 1 min. for HCPL-4506 Option 020 and HCNW4506
  **CSA Approved**
  **IEC / EN / DIN EN 60747-5-2 Approved**
  -$V_{IORM}$ = 560 Vpeak for HCPL-0466 Option 060
  -$V_{IORM}$ = 630 Vpeak for HCPL-4506 Option 060
  -$V_{IORM}$ = 891 Vpeak for HCPL-J456
  -$V_{IORM}$ = 1414 Vpeak for HCNW4506

### Applications

- **IPM isolation**
- **Isolated IGBT / MOSFET gate drive**
- **AC and brushless DC motor drives**
- **Industrial inverters**

*CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

## Selection Guide

| Package Type | Standard 8-Pin DIP (300 Mil) | White Mold 8-Pin DIP (300 Mil) | Small Outline SO8 | Widebody (400 Mil) | Hermetic* |
|---|---|---|---|---|---|
| Part Number | HCPL-4506 | HCPL-J456 | HCPL-0466 | HCNW4506 | HCPL-5300<br>HCPL-5301 |
| IEC/EN/DIN EN 60747-5-2 Approval | $V_{IORM}$ = 630 Vpeak (Option 060) | $V_{IORM}$ = 891 Vpeak | $V_{IORM}$ = 560 Vpeak (Option 060) | $V_{IORM}$ = 1414 Vpeak | — |

*Technical data for these products are on separate Avago publications.

## Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

HCPL-4506#XXXX

- 020 = UL 5000 V rms/1 minute Option** for HCPL-4506 Only.
- 060 = IEC/EN/DIN EN 60747-5-2 Option** for HCPL-4506/0466.
- 300 = Gull Wing Lead Option for HCPL-4506/J456, HCNW4506.
- 500 = Tape and Reel Packaging Option
- XXXE = Lead Free Option

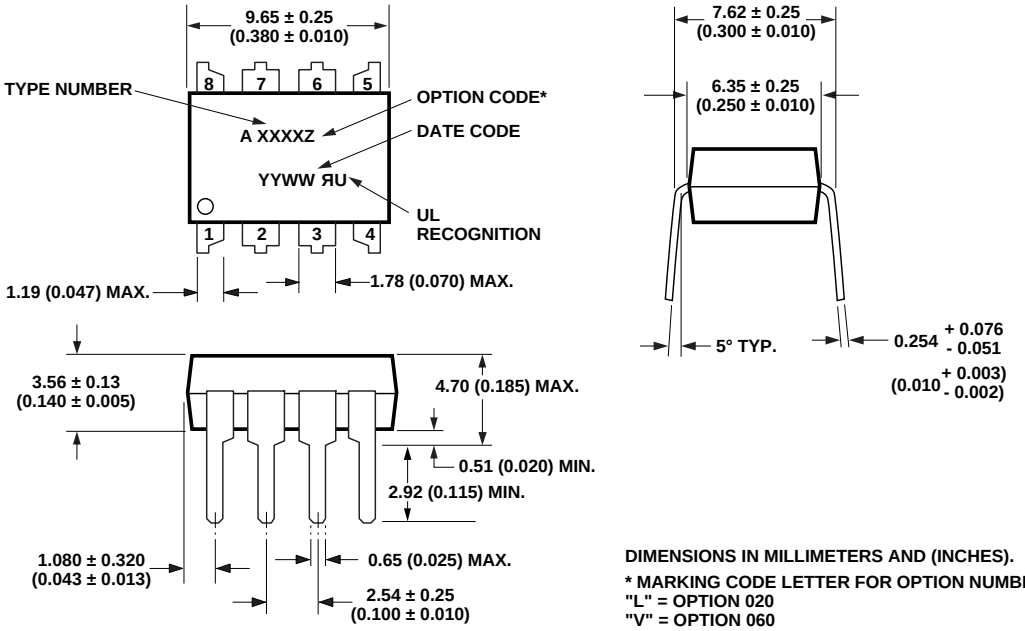
Option data sheets are available. Contact Avago sales representative or authorized distributor for information.

**Combination of Option 020 and Option 060 is not available.

Remarks: The notation "#" is used for existing products, while (new) products launched since 15th July 2001 and lead free option will use "-"

## Package Outline Drawings

### HCPL-4506 Outline Drawing

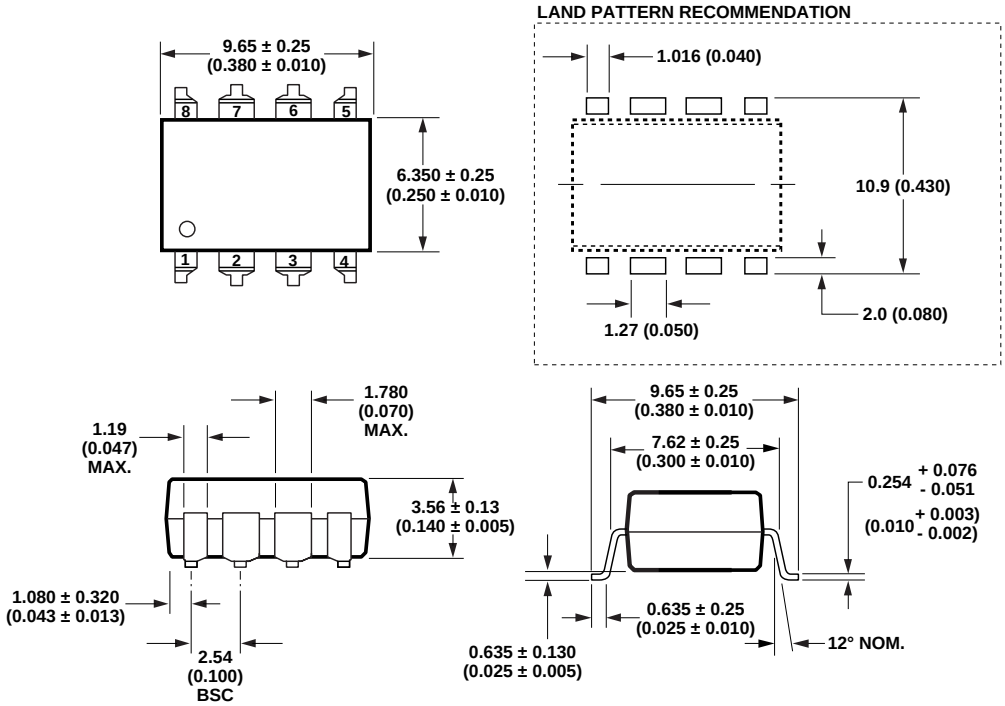



DIMENSIONS IN MILLIMETERS AND (INCHES).

* MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

### HCPL-4506 Gull Wing Surface Mount Option 300 Outline Drawing

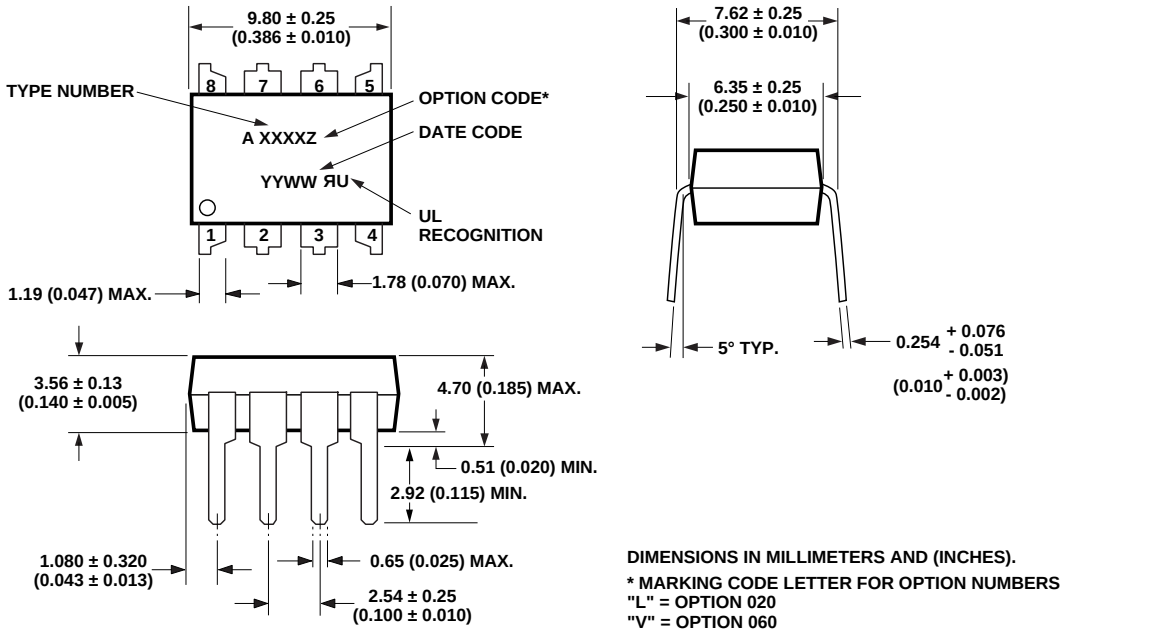



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

## Package Outline Drawings

### HCPL-J456 Outline Drawing

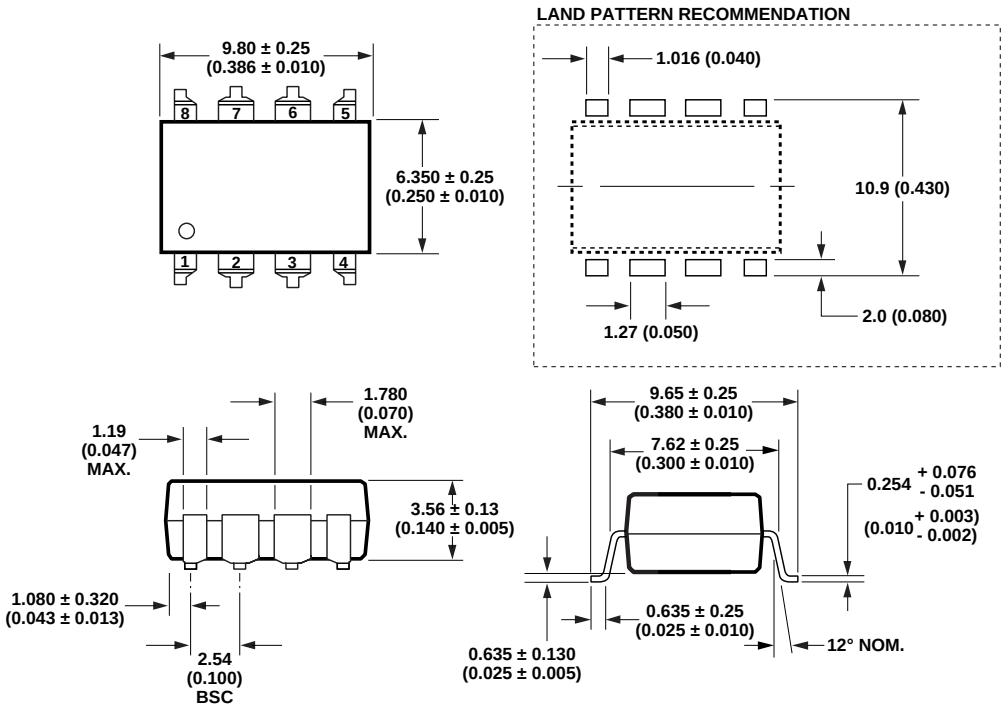



DIMENSIONS IN MILLIMETERS AND (INCHES).

* MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

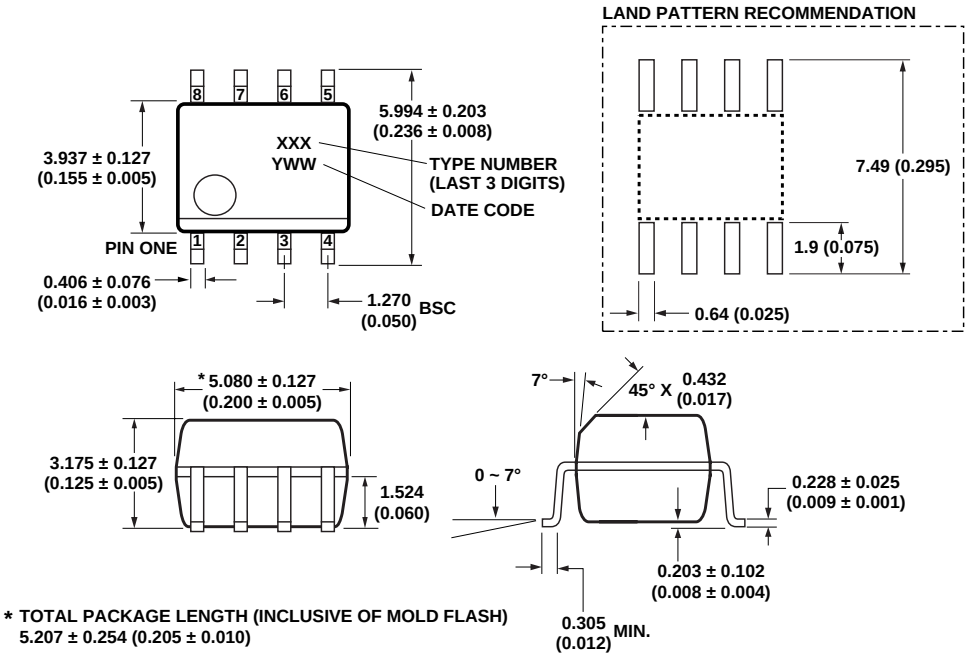
### HCPL-J456 Gull Wing Surface Mount Option 300 Outline Drawing




DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

## HCPL-0466 Outline Drawing (8-Pin Small Outline Package)

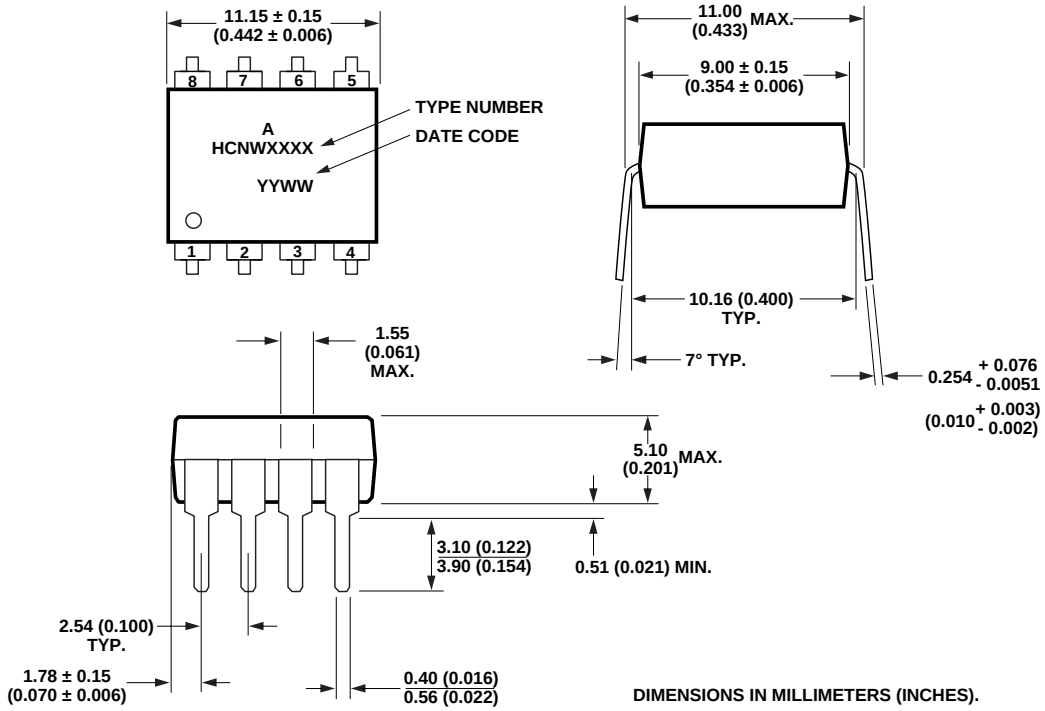



* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

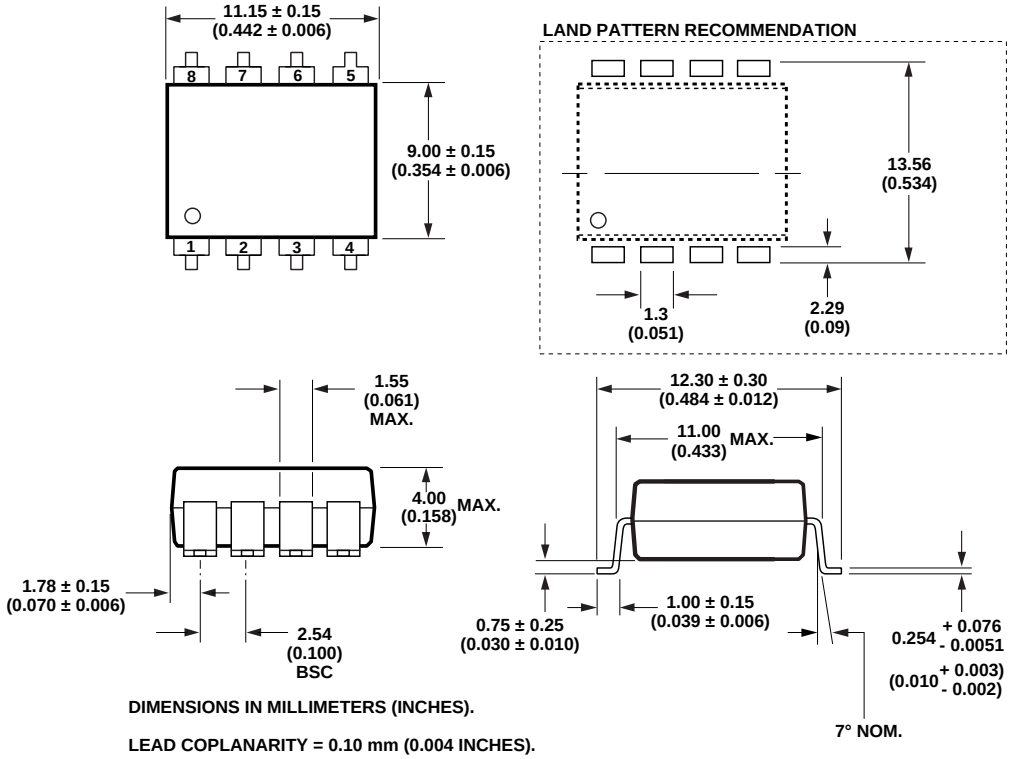
## HCNW4506 Outline Drawing (8-Pin Widebody Package)




DIMENSIONS IN MILLIMETERS (INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

## HCNW4506 Gull Wing Surface Mount Option 300 Outline Drawing

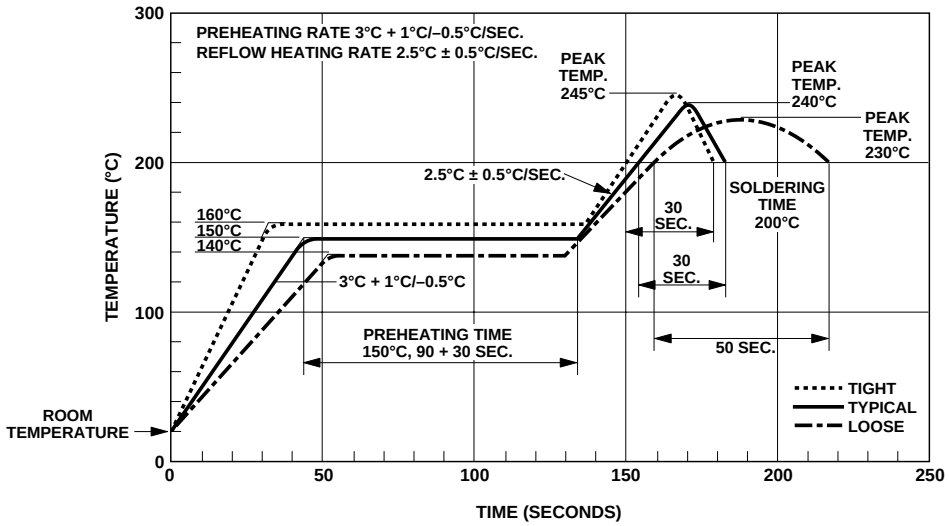



DIMENSIONS IN MILLIMETERS (INCHES).

LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

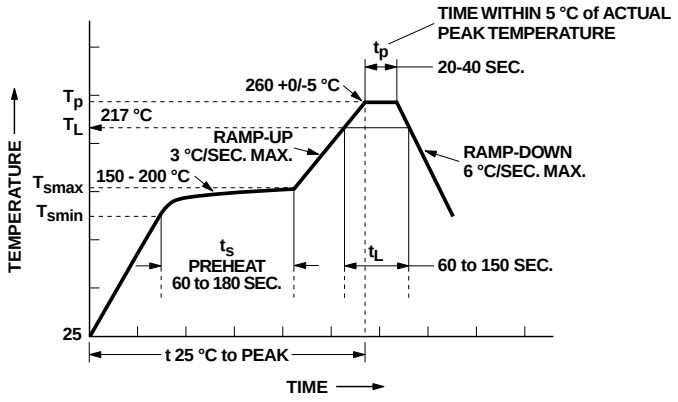
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

## Solder Reflow Temperature Profile




**Note: Use of non-chlorine-activated fluxes is highly recommended.**

## Recommended Pb-Free IR Profile




**NOTES:**
**THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.**
**$T_{smax}$ = 200 °C, $T_{smin}$ = 150 °C**

**Note: Use of non-chlorine-activated fluxes is highly recommended.**

**Regulatory Information**

The devices contained in this data sheet have been approved by the following agencies:

| Agency / Standard | | HCPL-4506 | HCPL-J456 | HCPL-0466 | HCNW4506 |
|---|---|---|---|---|---|
| **Underwriters Laboratories (UL)** Recognized under UL 1577, Component Recognized Program, Category FPQU2, File E55361 | UL 1577 | ✔ | ✔ | ✔ | ✔ |
| **Canadian Standards Association (CSA)** File CA88324 | Component Acceptance Notice #5 | ✔ | ✔ | ✔ | ✔ |
| **Verband Deutscher Electrotechniker (VDE)** | DIN VDE 0884 (June 1992) | ✔ | ✔ | | ✔ |
| **IEC / EN / DIN EN 60747-5-2** Approved under: IEC 60747-5-2:1997 + A1:2002 EN 60747-5-2:2001 + A1:2002 DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01 | | ✔ | ✔ | ✔ | ✔ |

**Insulation and Safety Related Specifications**

| | | Value | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **HCPL-4506** | **HCPL-J456** | **HCPL-0466** | **HCNW4506** | **Units** | **Conditions** |
| Minimum External Air Gap (External Clearance) | L(101) | 7.1 | 7.4 | 4.9 | 9.6 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (External Creepage) | L(102) | 7.4 | 8.0 | 4.8 | 10.0 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Minimum Internal Plastic Gap (Internal Clearance) | | 0.08 | 0.5 | 0.08 | 1.0 | mm | Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity. |
| Minimum Internal Tracking (Internal Creepage) | | NA | NA | NA | 4.0 | mm | Measured from input terminals to output terminals, along internal cavity. |
| Tracking Resistance (Comparative Tracing Index) | CTI | ≥175 | ≥175 | ≥175 | ≥200 | Volts | DIN IEC 112 / VDE 0303 Part 1 |
| Isolation Group | | IIIa | IIIa | IIIa | IIIa | | Material Group (DIN VDE 0110, 1 / 89, Table 1) |

All Avago data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered. There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

**IEC / EN / DIN EN 60747-5-2 Insulation Related Characteristics**

| Description | Symbol | HCPL-0466 Option 060 | HCPL-4506 Option 060 | HCPL-J456 | HCNW4506 | Unit |
|---|---|---|---|---|---|---|
| Installation classification per DIN VDE 0110/1.89, Table 1 | | | | | | |
| for rated mains voltage ≤150 V rms | | I-IV | I-IV | I-IV | I-IV | |
| for rated mains voltage ≤300 V rms | | I-III | I-IV | I-IV | I-IV | |
| for rated mains voltage ≤450 V rms | | | I-III | I-III | I-IV | |
| for rated mains voltage ≤600 V rms | | | | I-III | I-IV | |
| for rated mains voltage ≤1000 V rms | | | | | I-III | |
| Climatic Classification | | 55/100/21 | 55/100/21 | 55/100/21 | 55/100/21 | |
| Pollution Degree (DIN VDE 0110/1.89) | | 2 | 2 | 2 | 2 | |
| Maximum Working Insulation Voltage | $V_{IORM}$ | 560 | 630 | 891 | 1414 | $V_{peak}$ |
| Input to Output Test Voltage, Method b* $V_{IORM}$ x 1.875 = $V_{PR}$, 100% Production Test with $t_m$ = 1 sec, Partial Discharge < 5pC | $V_{PR}$ | 1050 | 1181 | 1670 | 2652 | $V_{peak}$ |
| Input to Output Test Voltage, Method a* $V_{IORM}$ x 1.5 = $V_{PR}$, Type and Sample Test, $t_m$ = 60 sec, Partial Discharge < 5pC | $V_{PR}$ | 840 | 945 | 1336 | 2121 | $V_{peak}$ |
| Highest Allowable Overvoltage* (Transient Overvoltage, $t_{ini}$ = 10 sec) | $V_{IOTM}$ | 4000 | 6000 | 6000 | 8000 | $V_{peak}$ |
| Safety Limiting Values – maximum values allowed in the event of a failure, also see Thermal Derating curve. | | | | | | |
| Case Temperature | $T_S$ | 150 | 175 | 175 | 150 | °C |
| Input Current | $I_{S\ INPUT}$ | 150 | 230 | 400 | 400 | mA |
| Output Power | $P_{S\ OUTPUT}$ | 600 | 600 | 600 | 700 | mW |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500 V | $R_S$ | $\geq 10^9$ | $\geq 10^9$ | $\geq 10^9$ | $\geq 10^9$ | Ω |

*Refer to the optocoupler section of the Designer's Catalog, under regulatory information (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

Note: These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Note: Insulation Characteristics are per IEC/EN/DIN EN 60747-5-2.

Note: Surface mount classification is Class A in accordance with CECC 00802.

**Absolute Maximum Ratings**

| Parameter | | Symbol | Min. | Max. | Units |
|---|---|---|---|---|---|
| Storage Temperature | | $T_S$ | -55 | 125 | °C |
| Operating Temperature | | $T_A$ | -40 | 100 | °C |
| Average Input Current[1] | | $I_{F(avg)}$ | | 25 | mA |
| Peak Input Current[2] (50% duty cycle, ≤1 ms pulse width) | | $I_{F(peak)}$ | | 50 | mA |
| Peak Transient Input Current (<1 μs pulse width, 300 pps) | | $I_{F(tran)}$ | | 1.0 | A |
| Reverse Input Voltage (Pin 3-2) | HCPL-4506, HCPL-0466 | $V_R$ | | 5 | Volts |
| | HCPL-J456, HCNW4506 | | | 3 | |
| Average Output Current (Pin 6) | | $I_{O(avg)}$ | | 15 | mA |
| Resistor Voltage (Pin 7) | | $V_7$ | -0.5 | $V_{CC}$ | Volts |
| Output Voltage (Pin 6-5) | | $V_O$ | -0.5 | 30 | Volts |
| Supply Voltage (Pin 8-5) | | $V_{CC}$ | -0.5 | 30 | Volts |
| Output Power Dissipation[3] | | $P_O$ | | 100 | mW |
| Total Power Dissipation[4] | | $P_T$ | | 145 | mW |
| Lead Solder Temperature (HCPL-4506, HCPL-J456) | | 260°C for 10 s, 1.6 mm below seating plane | | | |
| Lead Solder Temperature (HCNW4506) | | 260°C for 10 s (up to seating plane) | | | |
| Infrared and Vapor Phase Reflow Temperature (HCPL-0466 and Option 300) | | See **Package Outline Drawings** Section | | | |

**Recommended Operating Conditions**

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 30 | Volts |
| Output Voltage | $V_O$ | 0 | 30 | Volts |
| Input Current (ON) | $I_{F(on)}$ | 10 | 20 | mA |
| Input Voltage (OFF) | $V_{F(off)}$* | -5 | 0.8 | V |
| Operating Temperature | $T_A$ | -40 | 100 | °C |

*Recommended $V_{F(OFF)}$ = -3 V to 0.8 V for HCPL-J456, HCNW4506.

**Electrical Specifications**

Over recommended operating conditions unless otherwise specified:

$T_A$ = -40°C to +100°C, $V_{CC}$ = +4.5 V to 30 V, $I_{F(on)}$ = 10 mA to 20 mA, $V_{F(off)}$ = -5 V to 0.8 V†

| Parameter | Symbol | Device | Min. | Typ.* | Max. | Units | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|---|
| Current Transfer Ratio | CTR | | 44 | 90 | | % | $I_F$ = 10 mA, $V_O$ = 0.6 V | | 5 |
| Low Level Output Current | $I_{OL}$ | | 4.4 | 9.0 | | mA | $I_F$ = 10 mA, $V_O$ = 0.6 V | 1, 2 | |
| Low Level Output Voltage | $V_{OL}$ | | | 0.3 | 0.6 | V | $I_O$ = 2.4 mA | | |
| Input Threshold Current | $I_{TH}$ | HCPL-4506 HCPL-0466 HCNW4506 | | 1.5 | 5 | mA | $V_O$ = 0.8 V, $I_O$ = 0.75 mA | 1 | 16 |
| | | HCPL-J456 | | 0.6 | | | | | |
| High Level Output Current | $I_{OH}$ | | | 5 | 50 | µA | $V_F$ = 0.8 V | 3 | |
| High Level Supply Current | $I_{CCH}$ | | | 0.6 | 1.3 | mA | $V_F$ = 0.8 V, $V_O$ = Open | | 16 |
| Low Level Supply Current | $I_{CCL}$ | | | 0.6 | 1.3 | mA | $I_F$ = 10 mA, $V_O$ = Open | | 16 |
| Input Forward Voltage | $V_F$ | HCPL-4506 HCPL-0466 | | 1.5 | 1.8 | V | $I_F$ = 10 mA | 4 | |
| | | HCPL-J456 | 1.2 | 1.6 | 1.95 | | | 5 | |
| | | HCNW4506 | | 1.6 | 1.85 | | | | |
| Temperature Coefficient of Forward Voltage | $\Delta V_F/\Delta T_A$ | HCPL-4506 HCPL-0466 | | -1.6 | | mV/°C | $I_F$ = 10 mA | | |
| | | HCPL-J456 HCNW4506 | | -1.3 | | | | | |
| Input Reverse Breakdown Voltage | $BV_R$ | HCPL-4506 HCPL-0466 | 5 | | | V | $I_R$ = 10 µA | | |
| | | HCPL-J456 HCNW4506 | 3 | | | | $I_R$ = 100 µA | | |
| Input Capacitance | $C_{IN}$ | HCPL-4506 HCPL-0466 | | 60 | | pF | f = 1 MHz, $V_F$ = 0 V | | |
| | | HCPL-J456 HCNW4506 | | 72 | | | | | |
| Internal Pull-up Resistor | $R_L$ | | 14 | 20 | 25 | kΩ | $T_A$ = 25°C | | 12, 13 |
| Internal Pull-up Resistor Temperature Coefficient | $\Delta R_L/\Delta T_A$ | | | 0.014 | | kΩ/°C | | | |

*All typical values at 25°C, $V_{CC}$ = 15 V.

†$V_{F(off)}$ = -3 V to 0.8 V for HCPL-J456, HCNW4506.

**Switching Specifications ($R_L$ = 20 kΩ External)**

Over recommended operating conditions unless otherwise specified:
$T_A$ = -40°C to +100°C, $V_{CC}$ = +4.5 V to 30 V, $I_{F(on)}$ = 10 mA to 20 mA, $V_{F(off)}$ = -5 V to 0.8 V†

| Parameter | Symbol | Min. | Typ.* | Max. | Units | Test Conditions | | Fig. | Note |
|---|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time to Logic Low at Output HCPL-J456 | $T_{PHL}$ | 30 | 200 | 400 | ns | $C_L$ = 100 pF | $I_{F(on)}$ = 10 mA, $V_{F(off)}$ = 0.8 V, $V_{CC}$ = 15.0 V, $V_{THLH}$ = 2.0 V, $V_{THHL}$ = 1.5 V | 6, 8, 10-13 | 11, 14, 16 |
| | | | | 480 | | | | | |
| | | | 100 | | | $C_L$ = 10 pF | | | |
| Propagation Delay Time to High Output Level | $T_{PLH}$ | 270 | 400 | 550 | ns | $C_L$ = 100 pF | | | |
| | | | 130 | | | $C_L$ = 10 pF | | | |
| Pulse Width Distortion | PWD | | 200 | 450 | ns | $C_L$ = 100 pF | | | 20 |
| Propagation Delay Difference Between Any 2 Parts | $t_{PLH}$-$t_{PHL}$ | -150 | 200 | 450 | ns | | | | 17 |
| Output High Level Common Mode Transient Immunity | $\|CM_H\|$ | 15 | 30 | | kV/µs | $I_F$ = 0 mA, $V_O$ > 3.0 V | $V_{CC}$ = 15.0 V, $C_L$ = 100 pF, $V_{CM}$ = 1500 $V_{p-p}$ $T_A$ = 25°C | 7 | 18 |
| Output Low Level Common Mode Transient Immunity | $\|CM_L\|$ | 15 | 30 | | kV/µs | $I_F$ = 10 mA $V_O$ < 1.0 V | | | 19 |

**Switching Specifications ($R_L$ = Internal Pull-up)**

Over recommended operating conditions unless otherwise specified:
$T_A$ = -40°C to +100°C, $V_{CC}$ = +4.5 V to 30 V, $I_{F(on)}$ = 10 mA to 20 mA, $V_{F(off)}$ = -5 V to 0.8 V†

| Parameter | Symbol | Min. | Typ.* | Max. | Units | Test Conditions | | Fig. | Note |
|---|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time to Logic Low at Output HCPL-J456 | $t_{PHL}$ | 20 | 200 | 400 | ns | $I_{F(on)}$ = 10 mA, $V_{F(off)}$ = 0.8 V, $V_{CC}$ = 15.0 V, $C_L$ = 100 pF, $V_{THLH}$ = 2.0 V, $V_{THHL}$ = 1.5 V | | 6, 9 | 11-14, 16 |
| | | | | 485 | | | | | |
| Propagation Delay Time to High Output Level | $t_{PLH}$ | 220 | 450 | 650 | ns | | | | |
| Pulse Width Distortion | PWD | | 250 | 500 | ns | | | | 20 |
| Propagation Delay Difference Between Any 2 Parts | $t_{PLH}$-$t_{PHL}$ | -150 | 250 | 500 | ns | | | | 17 |
| Output High Level Common Mode Transient Immunity | $\|CM_H\|$ | | 30 | | kV/µs | $I_F$ = 0 mA, $V_O$ > 3.0 V | $V_{CC}$ = 15.0 V, $C_L$ = 100 pF, $V_{CM}$ = 1500 $V_{p-p}$, $T_A$ = 25°C | 7 | 18 |
| Output Low Level Common Mode Transient Immunity | $\|CM_L\|$ | | 30 | | kV/µs | $I_F$ = 16 mA, $V_O$ < 1.0 V | | | 19 |
| Power Supply Rejection | PSR | | 1.0 | | $V_{p-p}$ | Square Wave, $t_{RISE}$, $t_{FALL}$ > 5 ns, no bypass capacitors | | | 16 |

*All typical values at 25°C, $V_{CC}$ = 15 V.
†$V_{F(off)}$ = -3 V to 0.8 V for HCPL-J456, HCNW4506.

**Package Characteristics**

Over recommended temperature ($T_A$ = -40°C to 100°C) unless otherwise specified.

| Parameter | Sym. | Device | Min. | Typ.* | Max. | Units | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|---|
| Input-Output Momentary Withstand Voltage† | $V_{ISO}$ | HCPL-4506 HCPL-0466 | 3750 | | | V rms | RH < 50% t = 1 min. $T_A$ = 25°C | | 6,7,10 |
| | | HCPL-J456 | 3750 | | | | | | 6,8,10 |
| | | HCPL-4506 Option020 | 5000 | | | | | | 6,9, 15 |
| | | HCNW4506 | 5000 | | | | | | 6,9,10 |
| Resistance (Input-Output) | $R_{I-O}$ | HCPL-4506 HCPL-J456 HCPL-0466 | | $10^{12}$ | | Ω | $V_{I-O}$ = 500 Vdc | | 6 |
| | | HCNW4506 | $10^{12}$ | $10^{13}$ | | | | | |
| Capacitance (Input-Output) | $C_{I-O}$ | HCPL-4506 HCPL-0466 | | 0.6 | | pF | f = 1 MHz | | 6 |
| | | HCPL-J456 | | 0.8 | | | | | |
| | | HCNW4506 | | 0.5 | | | | | |

*All typical values at 25°C, $V_{CC}$ = 15 V.

†The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics Table (if applicable), your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage," publication number 5963-2203E.

**Notes:**

1. Derate linearly above 90°C free-air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 90°C free-air temperature at a rate of 1.6 mA/°C.
3. Derate linearly above 90°C free-air temperature at a rate of 3.0 mW/°C.
4. Derate linearly above 90°C free-air temperature at a rate of 4.2 mW/°C.
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current ($I_O$) to the forward LED input current ($I_F$) times 100.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥4500 V rms for 1 second (leakage detection current limit, $I_{I-O}$ ≤5 μA).
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 second (leakage detection current limit, $I_{i-o}$ ≤ 5 μA).
9. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (leakage detection current limit, $I_{I-O}$ ≤ 5 μA).
10. This test is performed before the 100% Production test shown in the IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics Table, if applicable.
11. Pulse: f = 20 kHz, Duty Cycle = 10%.
12. The internal 20 kΩ resistor can be used by shorting pins 6 and 7 together.
13. Due to tolerance of the internal resistor, and since propagation delay is dependent on the load resistor value, performance can be improved by using an external 20 kΩ 1% load resistor. For more information on how propagation delay varies with load resistance, see Figure 8.
14. The $R_L$ = 20 kΩ, $C_L$ = 100 pF load represents a typical IPM (Intelligent Power Module) load.
15. See Option 020 data sheet for more information.
16. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 can improve performance by filtering power supply line noise.
17. The difference between $t_{PLH}$ and $t_{PHL}$ between any two devices under the same test condition. (See IPM Dead Time and Propagation Delay Specifications section.)
18. Common mode transient immunity in a Logic High level is the maximum tolerable $dV_{CM}/dt$ of the common mode pulse, $V_{CM}$, to assure that the output will remain in a Logic High state (i.e., $V_O$ > 3.0 V).
19. Common mode transient immunity in a Logic Low level is the maximum tolerable $dV_{CM}/dt$ of the common mode pulse, $V_{CM}$, to assure that the output will remain in a Logic Low state (i.e., $V_O$ < 1.0 V).
20. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.

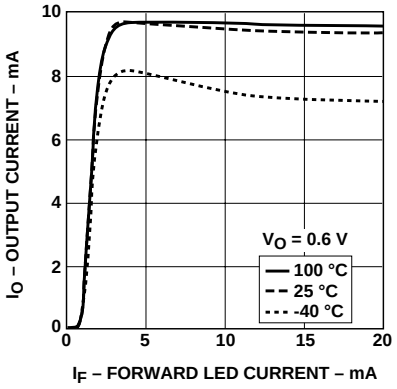



Figure 1. Typical transfer characteristics.

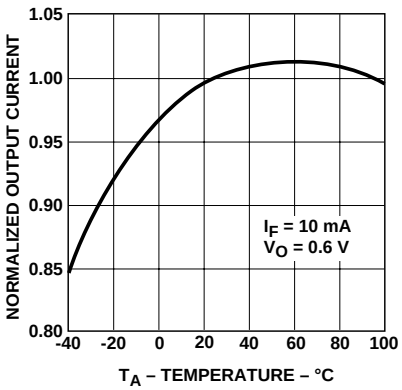



Figure 2. Normalized output current vs. temperature.

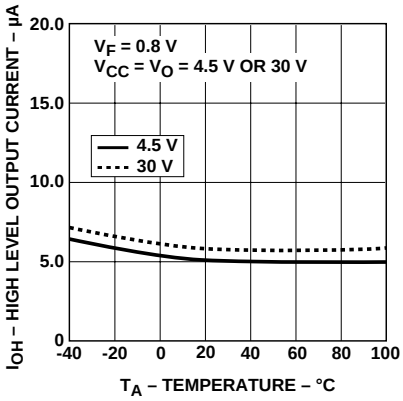



Figure 3. High level output current vs. temperature.

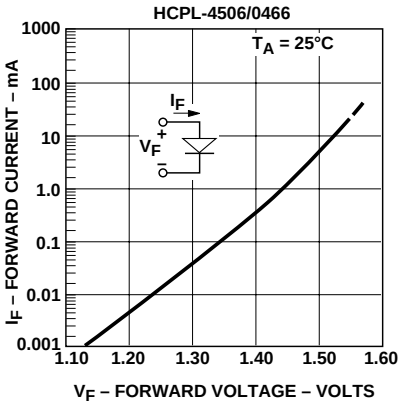



Figure 4. HCPL-4506 and HCPL-0466 input current vs. forward voltage.

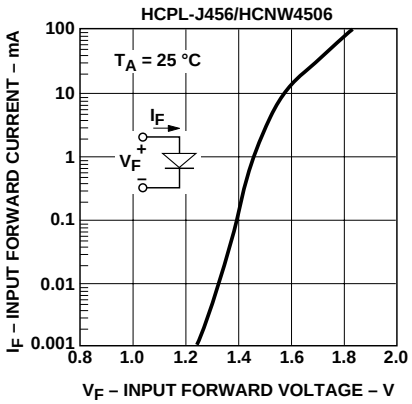



Figure 5. HCPL-J456 and HCNW4506 input current vs. forward voltage.

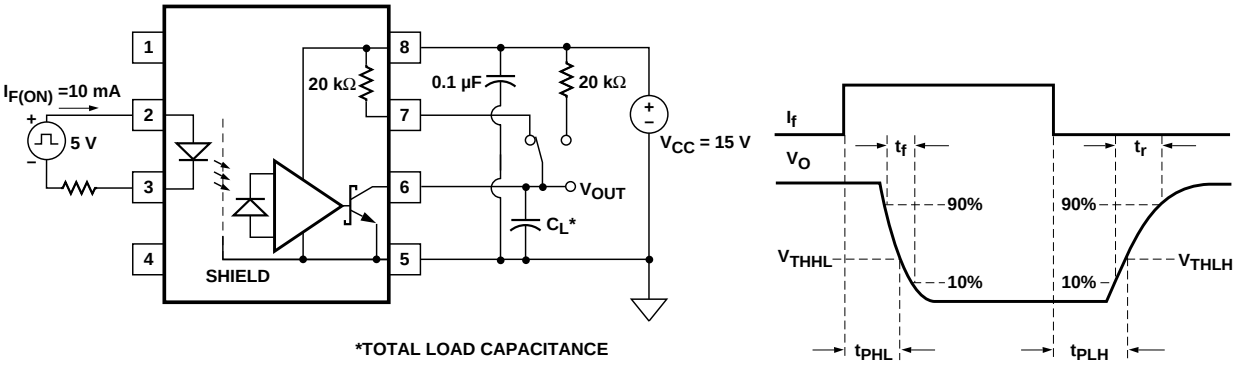



Figure 6. Propagation delay test circuit.

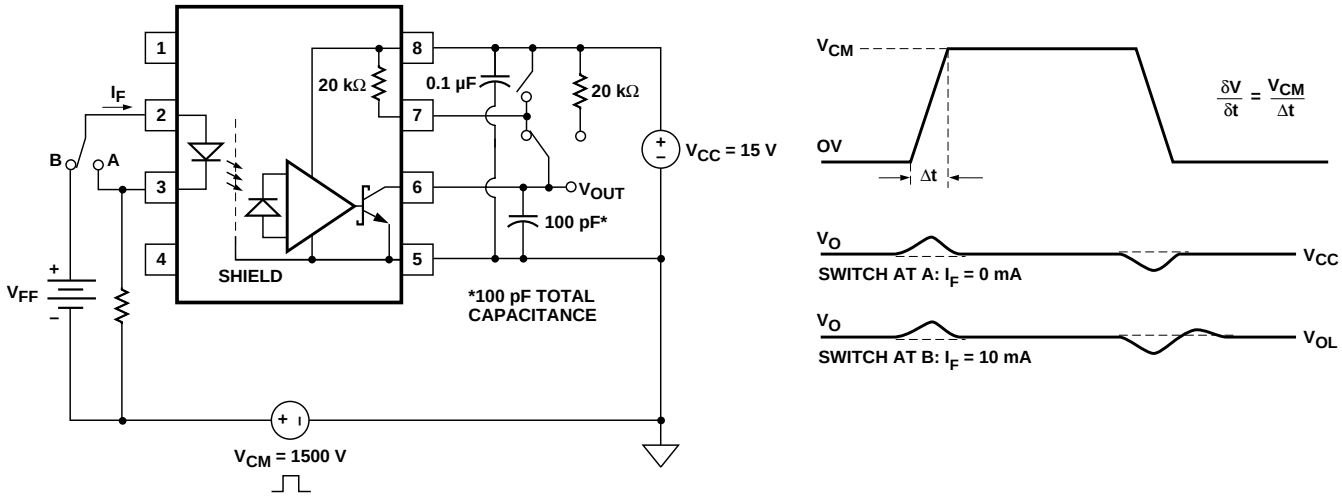



**Figure 7. CMR test circuit. Typical CMR waveform.**

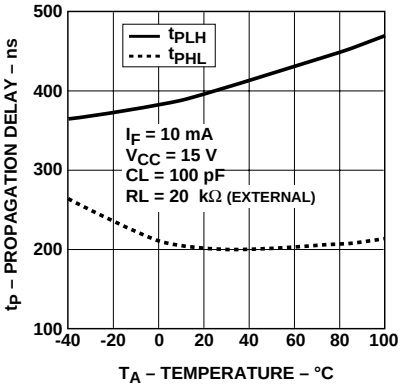



**Figure 8. Propagation delay with external 20 kΩ RL vs. temperature.**

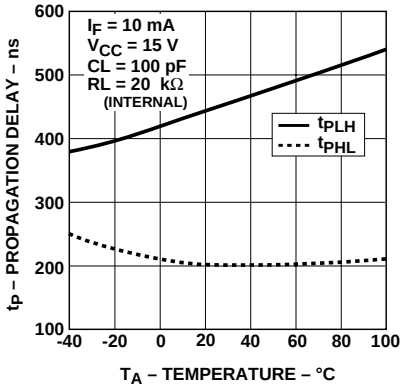



**Figure 9. Propagation delay with internal 20 kΩ RL vs. temperature.**

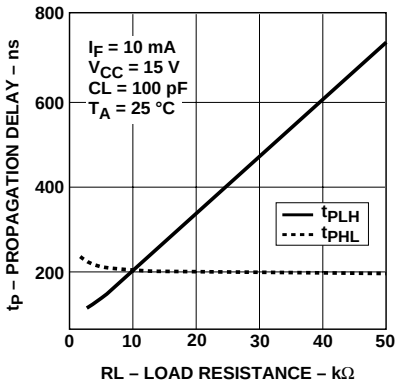



**Figure 10. Propagation delay vs. load resistance.**

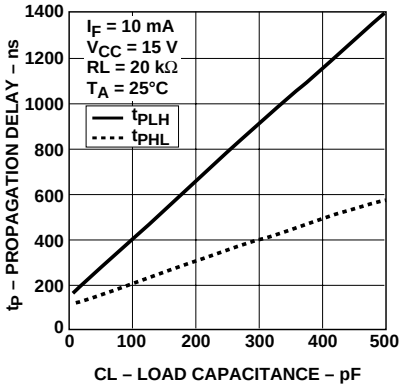



**Figure 11. Propagation delay vs. load capacitance.**

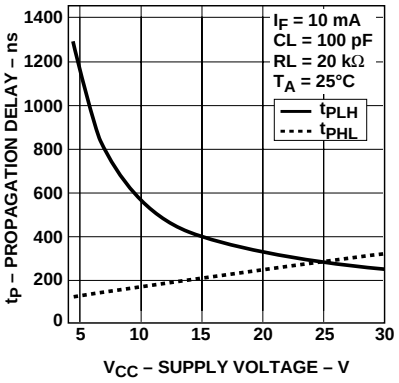



**Figure 12. Propagation delay vs. supply voltage.**

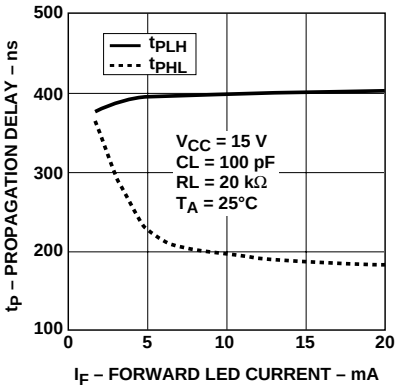



**Figure 13. Propagation delay vs. input current.**

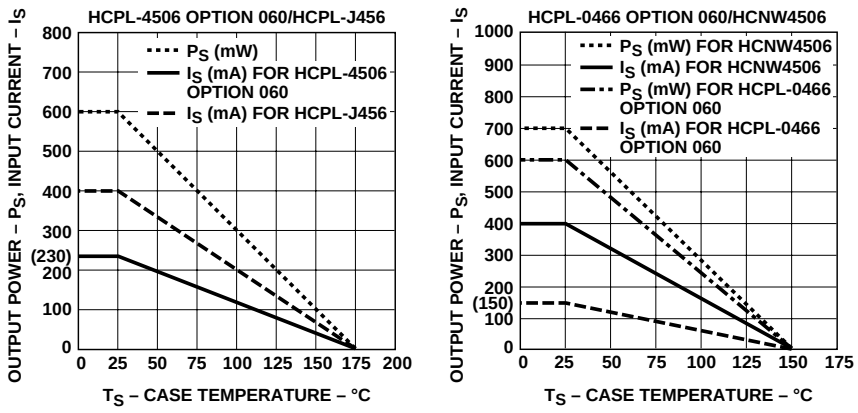



**Figure 14. Thermal derating curve, dependence of safety limiting value with case temperature per IEC / EN / DIN EN 60747-5-2.**

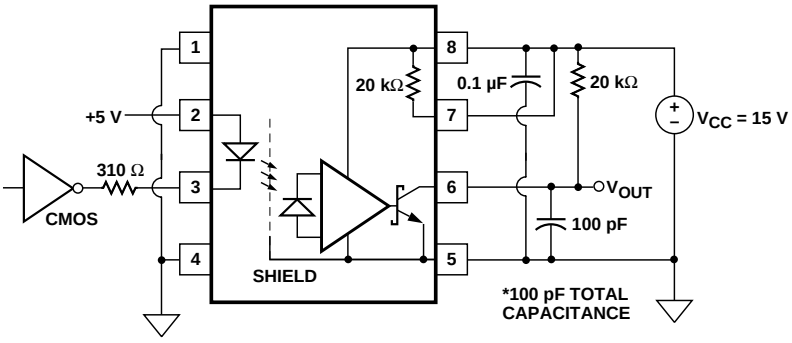



**Figure 15. Recommended LED drive circuit.**

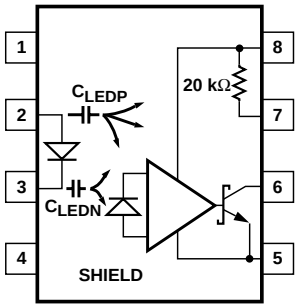



**Figure 16. Optocoupler input to output capacitance model for unshielded optocouplers.**

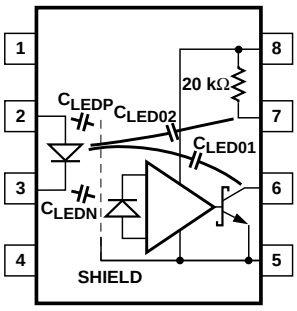



**Figure 17. Optocoupler input to output capacitance model for shielded optocouplers.**

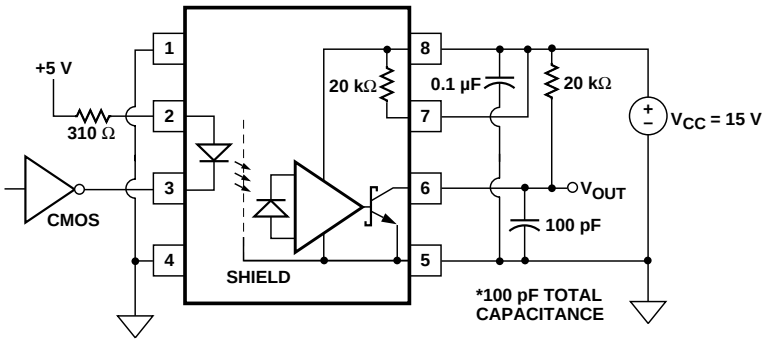



**Figure 18. LED drive circuit with resistor connected to LED anode (not recommended).**

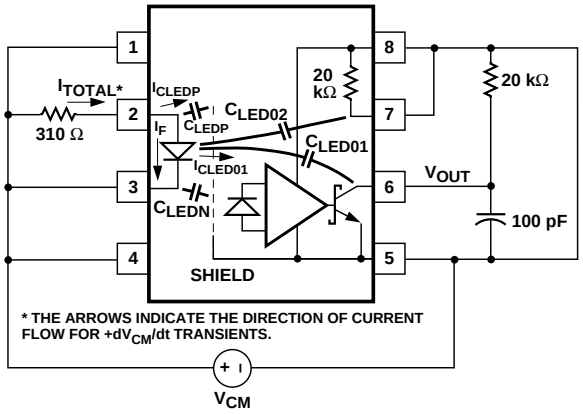



**Figure 19. AC equivalent circuit for Figure 18 during common mode transients.**

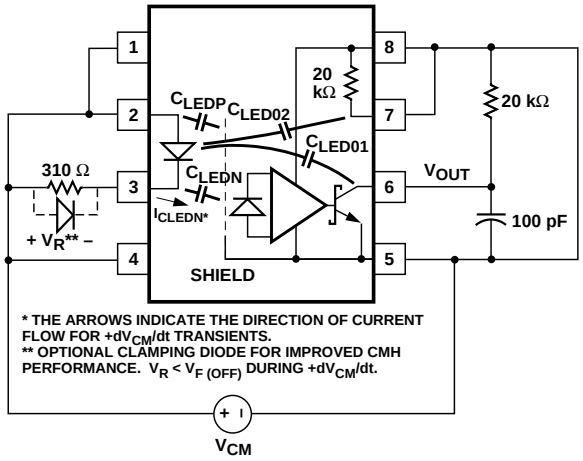



**Figure 20. AC equivalent circuit for Figure 15 during common mode transients.**

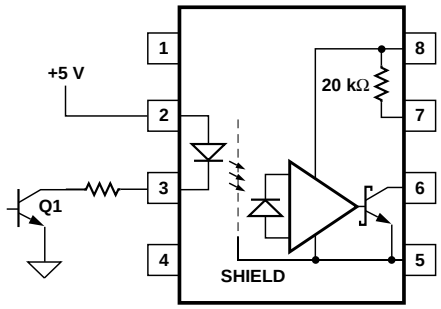



**Figure 21. Not recommended open collector LED drive circuit.**

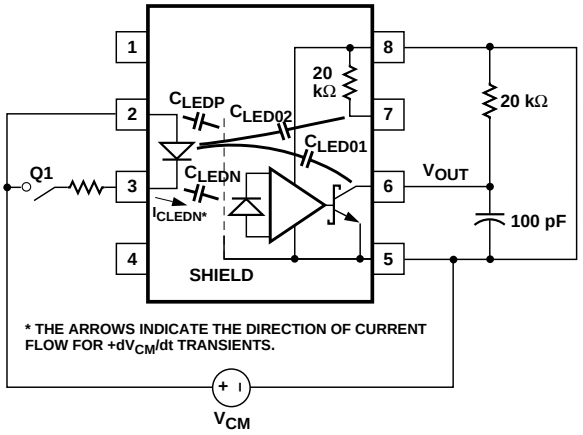



**Figure 22. AC Equivalent circuit for Figure 21 during common mode transients.**

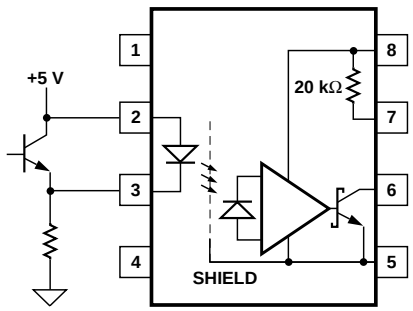



**Figure 23. Recommended LED drive circuit for ultra high CMR.**

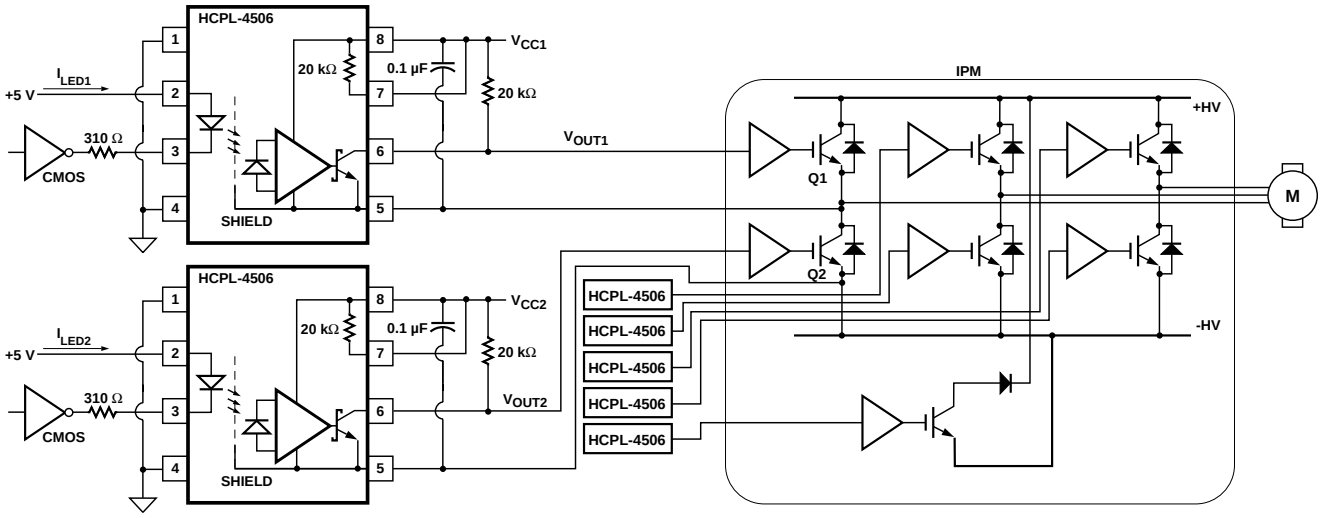
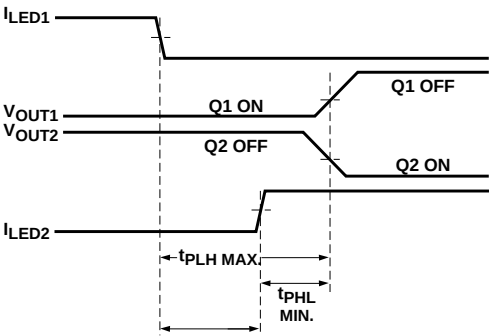



**Figure 24. Typical application circuit.**

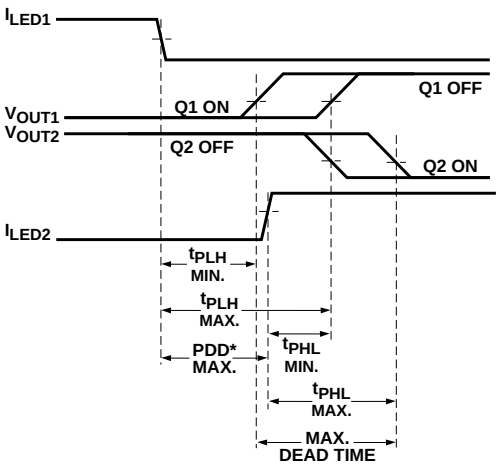



**PDD* MAX. =**
**$(t_{PLH}-t_{PHL})$ MAX. = $t_{PLH}$ MAX. - $t_{PHL}$ MIN.**

***PDD = PROPAGATION DELAY DIFFERENCE**

**NOTE: THE PROPAGATION DELAYS USED TO CALCULATE PDD ARE TAKEN AT EQUAL TEMPERATURES.**

**Figure 25. Minimum LED skew for zero dead time.**




**MAXIMUM DEAD TIME (DUE TO OPTOCOUPLER)**
**= $(t_{PLH\ MAX.} - t_{PLH\ MIN.}) + (t_{PHL\ MAX.} - t_{PHL\ MIN.})$**
**= $(t_{PLH\ MAX.} - t_{PHL\ MIN.}) - (t_{PLH\ MIN.} - t_{PHL\ MAX.})$**
**= PDD* MAX. - PDD* MIN.**

***PDD = PROPAGATION DELAY DIFFERENCE**

**NOTE: THE PROPAGATION DELAYS USED TO CALCULATE THE MAXIMUM DEAD TIME ARE TAKEN AT EQUAL TEMPERATURES.**

**Figure 26. Waveforms for dead time calculation.**

### LED Drive Circuit Considerations for Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 16. The HCPL-4506 series improve CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and the optocoupler output pins and output ground as shown in Figure 17. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 15), can achieve 15 kV/µs CMR while minimizing component complexity. Note that a CMOS gate is recommended in Figure 15 to keep the LED off when the gate is in the high state.

Another cause of CMR failure for a shielded optocoupler is direct coupling to the optocoupler output pins through $C_{LEDO1}$ and $C_{LEDO2}$ in Figure 17. Many factors influence the effect and magnitude of the direct coupling including: the use of an internal or external output pull-up resistor, the position of the LED current setting resistor, the connection of the unused input package pins, and the value of the capacitor at the optocoupler output ($C_L$).

Techniques to keep the LED in the proper state and minimize the effect of the direct coupling are discussed in the next two sections.

### CMR with the LED On ($CMR_L$)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. The recommended minimum LED current of 10 mA provides adequate margin over the maximum $I_{TH}$ of 5.0 mA (see Figure 1) to achieve 15 kV/µs CMR. Capacitive coupling is higher when the internal load resistor is used (due to $C_{LEDO2}$) and an $I_F$ = 16 mA is required to obtain 10 kV/µs CMR.

The placement of the LED current setting resistor effects the ability of the drive circuit to keep the LED on during transients and interacts with the direct coupling to the optocoupler output. For example, the LED resistor in Figure 18 is connected to the anode. Figure 19 shows the AC equivalent circuit for Figure 18 during common mode transients. During a +dVcm/dt in Figure 19, the current available at the LED anode (Itotal) is limited by the series resistor. The LED current ($I_F$) is reduced from its DC value by an amount equal to the current that flows through $C_{LEDP}$ and $C_{LEDO1}$. The situation is made worse because the current through $C_{LEDO1}$ has the effect of trying to pull the output high (toward a CMR failure) at the same time the LED current is being reduced. For this reason, the recommended LED drive circuit (Figure 15) places the current setting resistor in series with the LED cathode. Figure 20 is the AC equivalent circuit for Figure 15 during common mode transients. In this case, the LED current is not reduced during a +dVcm/dt transient because the current flowing through the package capacitance is supplied by the power supply. During a -dVcm/dt transient, however, the LED current is reduced by the amount of current flowing through $C_{LEDN}$. But, better CMR performance is achieved since the current flowing in $C_{LEDO1}$ during a negative transient acts to keep the output low.

Coupling to the LED and output pins is also affected by the connection of pins 1 and 4. If CMR is limited by perturbations in the LED on current, as it is for the recommended drive circuit (Figure 15), pins 1 and 4 should be connected to the input circuit common. However, if CMR performance is limited by direct coupling to the output when the LED is off, pins 1 and 4 should be left unconnected.

### CMR with the LED Off ($CMR_H$)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a +dVcm/dt transient in Figure 20, the current flowing through $C_{LEDN}$ is supplied by the parallel combination of the LED and series resistor. As long as the voltage developed across the resistor is less than $V_{F(OFF)}$ the

LED will remain off and no common mode failure will occur. Even if the LED momentarily turns on, the 100 pF capacitor from pins 6-5 will keep the output from dipping below the threshold. The recommended LED drive circuit (Figure 15) provides about 10 V of margin between the lowest optocoupler output voltage and a 3 V IPM threshold during a 15 kV/µs transient with $V_{CM}$ = 1500 V. Additional margin can be obtained by adding a diode in parallel with the resistor, as shown by the dashed line connection in Figure 20, to clamp the voltage across the LED below $V_{F(OFF)}$.

Since the open collector drive circuit, shown in Figure 21, cannot keep the LED off during a +dVcm/dt transient, it is not desirable for applications requiring ultra high $CMR_H$ performance. Figure 22 is the AC equivalent circuit for Figure 21 during common mode transients. Essentially all the current flowing through $C_{LEDN}$ during a +dVcm/dt transient must be supplied by the LED. $CMR_H$ failures can occur at dV/dt rates where the current through the LED and $C_{LEDN}$ exceeds the input threshold. Figure 23 is an alternative drive circuit which does achieve ultra high CMR performance by shunting the LED in the off state.

### IPM Dead Time and Propagation Delay Specifications

The HCPL-4506 series include a Propagation Delay Difference specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 24) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time the designer must consider the propagation delay characteristics of the optocoupler as well as the characteristics of the IPM IGBT gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the IPM IGBT gate drive circuit can be analyzed in the same way) it is important to know the minimum and maximum turn-on ($t_{PHL}$) and turn-off ($t_{PLH}$) propagation delay specifications, preferably over the desired operating temperature range.

The limiting case of zero dead time occurs when the input to Q1 turns off at the same time that the input to Q2 turns on. This case determines the minimum delay between LED1 turn-off and LED2 turn-on, which is related to the worst case optocoupler propagation delay waveforms, as shown in Figure 25. A minimum dead time of zero is achieved in Figure 25 when the signal to turn on LED2 is delayed by ($t_{PLH\ max}$ - $t_{PHL\ min}$) from the LED1 turn off. Note that the propagation delays used to calculate PDD are taken at equal temperatures since the optocouplers under consideration are typically mounted in close proximity to each other. (Specifically, $t_{PLH\ max}$ and $t_{PHL\ min}$ in the previous equation are not the same as the $t_{PLH\ max}$ and $t_{PHL\ min}$, over the full operating temperature range, specified in the data sheet.) This delay is the maximum value for the propagation delay difference specification which is specified at 450 ns for the HCPL-4506 series over an operating temperature range of -40°C to 100°C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time occurs in the highly unlikely case where one optocoupler with the fastest $t_{PLH}$ and another with the slowest $t_{PHL}$ are in the same inverter leg. The maximum dead time in this case becomes the sum of the spread in the $t_{PLH}$ and $t_{PHL}$ propagation delays as shown in Figure 26. The maximum dead time is also equivalent to the difference between the maximum and minimum propagation delay difference specifications. The maximum dead time (due to the optocouplers) for the HCPL-4506 series is 600 ns (= 450 ns - (-150 ns) ) over an operating temperature range of -40°C to 100°C.

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**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